Weekly Meetings Report

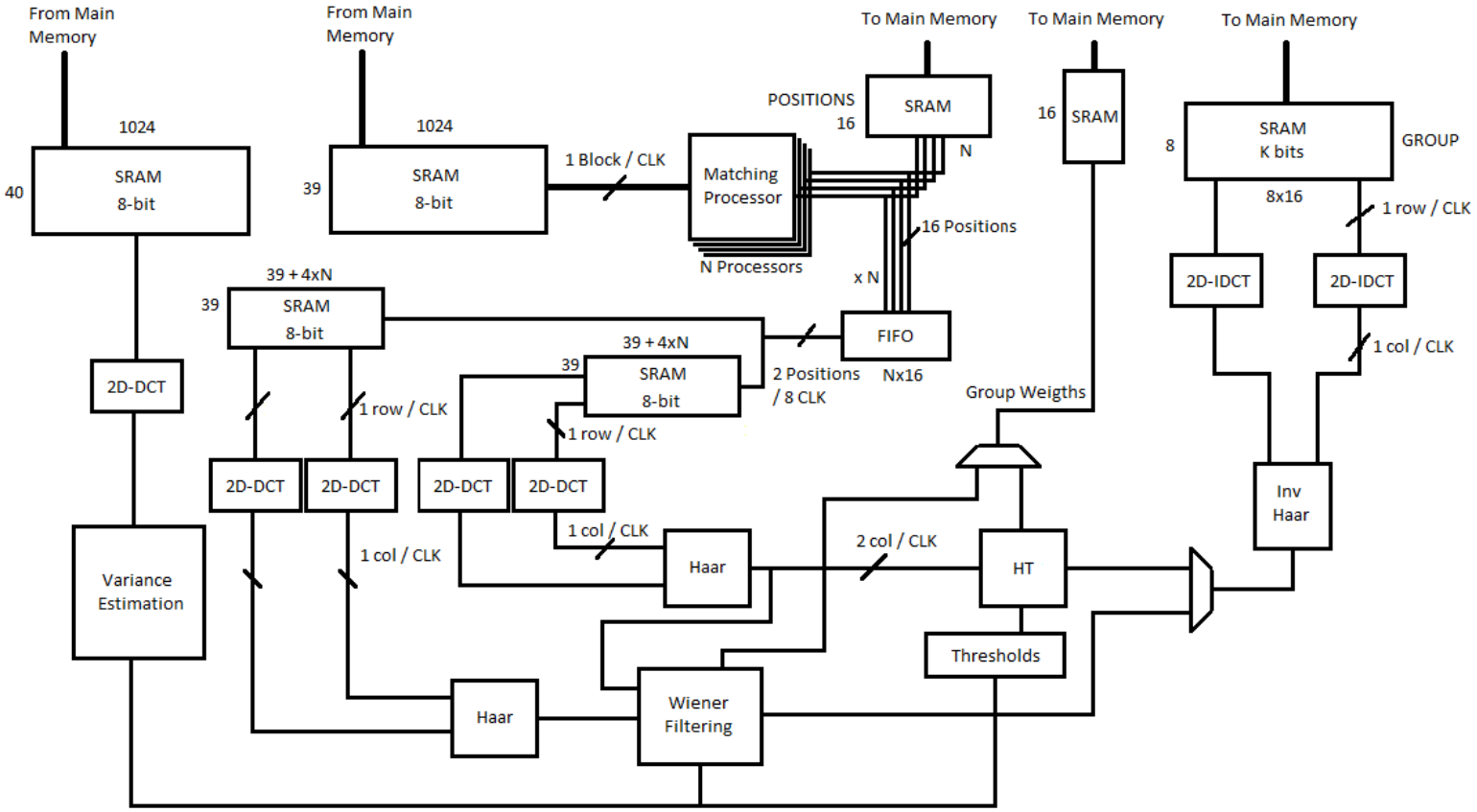
11 March 2015

Discussed Topics

1. ***System Architecture***
   The first draft of the system architecture was developed, with the previous discussed options being defined. The DCT is applied in the pipeline and not pre-computed for all the image, which has the main disadvantage of computing the DCT of the same block more than one time. However, in order to store the DCT of each block, a lot of memory would be necessary, which would require the use of external memory. Therefore, this implementation has the huge advantage of reducing the number of accesses to external memory, which are slow. The other main decision was the use of the ℓ_1 norm, instead of the ℓ_2 norm. Further testing in MATLAB revealed that the change in the norm wouldn't be a problem for the overall performance of the algorithm. Hence, for the hardware implementation, the ℓ_1 norm will be used, which is faster than the ℓ_2 norm, as it doesn't need multiplications. The proposed architecture can be found annexed to this report.
2. ***Haar Transform***
   Initially, the Haar transform block needed to wait for the data outputted by the DCT module, which meant breaking the pipeline. However, Professor Li suggested that some more effort should be put into trying not to break the pipeline. After a more careful evaluation, it was verified that by using 2 DCT modules in parallel, i.e., computing the DCT of two blocks at the same time, the Haar transform could be applied to the available data, without breaking the pipeline.
3. ***Wiener Filter***
   The Wiener Filter is the most complex block of the architecture, because it needs three multipliers and a division. The division is also the most complex operation to be implemented in the whole architecture.
4. ***Noise Estimation***
   Regarding the noise estimation, in MATLAB the estimator used is the MAD estimator, which consist of the multiplication of a constant by the median value of the high frequency coefficients of the image in transform domain. In order to compute the median in hardware, Professor Li suggested an histogram based approach, where the values of the coefficients are calculated and placed in the respective bin of the histogram. When all the image is processed, the median value is found by summing the counts of the bins of the histogram and stopping at the middle of the number of samples.

Next tasks

1. ***Start developing the architecture***
   For next week the plan is to begin coding in verilog the various blocks of the architecture, starting with the hard thresholding part of the algorithm.


From Main Memory
From Main Memory
To Main Memory
To Main Memory
To Main Memory
1024
40
SRAM 8-bit
1024
39
SRAM 8-bit
1 Block / CLK
Matching Processor
N Processors
POSITIONS 16
SRAM
N
16
SRAM
8
SRAM K bits
GROUP
8x16
1 row / CLK
16 Positions
x N
39 + 4xN
39
SRAM 8-bit
FIFO
Nx16
2 Positions / 8 CLK
2D-IDCT
2D-IDCT
1 col / CLK
2D-DCT
39 + 4xN
39
SRAM 8-bit
1 row / CLK
1 row / CLK
Group Weigths
2D-DCT
2D-DCT
2D-DCT
2D-DCT
Inv Haar
1 col / CLK
1 col / CLK
2 col / CLK
Variance Estimation
Haar
HT
Thresholds
Haar
Wiener Filtering