Weekly Meetings Report

19 March 2015

Discussed Topics

1. ***Work Development***
   The current state of the architecture development was discussed. The implementation of the matching processor is complete, with its correct behavior validated in a verilog testbench. The results of the testbench were compared with the block matching done in MATLAB and a 100% correctness was verified. For the remaining blocks, the DCT, Haar and Hard Thresholding, are already completed and validated individually.
2. ***Memory Access***
   Memory access to the RAM available on the ZYNQ board was explained by Mino Won. There are various AXI buses on the board, with different speeds, and the plan is to use the slower one and the ARM processor on chip to write on a register in the system, signaling that the image is placed in RAM. Then, the system will access the memory via the faster AXI bus, reading part of the image to SRAM inside the system.

Next tasks

1. ***Continue Architecture Development***
   For next week the plan is to continue the development of the architecture, focusing on finishing the denoising path implementation and validation.