Weekly Meetings Report

27 March 2015

Discussed Topics

1. ***Work Development***
   The current state of the architecture development was discussed. The implementation of the denoising path is complete, with its correct behavior verified by comparison between the verilog testbench and the MATLAB code.

Next tasks

1. ***Continue Architecture Development***
   For next week the plan is to continue the development of the architecture, focusing on the memory access to the DDR3 RAM on board, including the respective control and AXI protocol modules.