# Weekly Report

Week 7: 30/03/2015 - 03/04/2015

## Work Developed

This week, research was done on the AXI Interface Protocol in order to choose the most suitable variant for the memory access in the system. The AXI 4 Protocol is a Master - Slave Protocol and supports 3 types of interfaces: the AXI Lite Interface, AXI Memory Mapped and AXI Stream. The Lite interface is used when small amounts of data are transferred and it uses regular registers to store that data (typically 32 bit registers). This interface is used in the system as a slave, to enable the CPU to access the control and status registers, in order to issue the start of the denoising process and to know when it has finished. Then, for the actual image data transfer, as the system needs to fetch data frequently, an AXI Master is necessary. This master uses the Memory Mapped interface, allowing data to be transferred directly from RAM to the system memory.

## Challenges

The main challenge with choosing the AXI Interface was to ensure that the data transfers can be completed in enough time without jeopardizing the run-time of the algorithm.

## Next Tasks

Next week, work will be focused on development of verilog code for the AXI Master memory interface.

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