Weekly Report

Week 8: 06/04/2015 - 10/04/2015

Work Developed

This week, the AXI Master verilog code was developed. The code was developed by professor Li's PhD student Mino Won, and it was further adapted to meet the demands of the BM3D system. The developed module can access any address from the 4GB address space of the ZYNQ device, including the DDR3 controller which is used to access RAM where the image is stored. The module acts as the Master in the AXI transactions, which means the data transfers are initiated by the BM3D module itself, instead of the CPU.

Challenges

The main challenge in developing the AXI verilog code was making the necessary changes to Mino's code in order to adapt the module to the memories and data sizes of the BM3D module.

Next Tasks

Next week, work will be focused on development of the verilog code for the control logic of the system.

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