Weekly Report

Week 9: 13/04/2015 - 17/04/2015

Work Developed

This week, the control logic for the system was developed. It consists of 9 finite state machines, each with its own module:

1. This module is responsible for the control of the next neighborhood memory, which stores the data for the next image neighborhood to be processed.
2. This module loads the image data from a buffer memory, necessary to hold the image data between the block matching and denoising processes, to the memory inside the denoising pipeline.
3. This module is responsible for the control of the memory that stores the weights of each group (one weight per group).
4. This module is responsible for the control of the memory that stores the positions of each patch of each group (16 x,y positions per group).
5. This module is responsible for controlling the AXI Master interface which writes the position and weight data to RAM.
6. This module is responsible for controlling the AXI Master which writes the noise-free image data to RAM.
7. This module is responsible for controlling the output memory that holds the image data, in order to only store correct data that outputs from the denoising pipeline.
8. This module controls a flag that signals when the processing of a neighborhood has finished.
9. This module is the master control, which is responsible for controlling all the other control modules, as well as the internal control logic of the array of matching processors and the denoising pipeline. It also controls the AXI Master Interface which reads image data from RAM to on system memory.

Challenges

The main challenge in developing the control logic was debugging the whole system, as the AXI Slave Interfaces that need to answer to the requests of the Masters are not developed and thus are difficult to simulate with a testbench.

Next Tasks

Next week, work will be focused on development of the C code for the ARM CPU that operates in parallel with the BM3D system.

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