Weekly Report

Week 3: 02/03/2015 - 06/03/2015

Work Developed

In this week, work was focused on starting the development of the system level architecture of the system. It included the definition of the various blocks necessary for the implementation of the BM3D algorithm, such as the DCT and Haar transforms, the Matching processor (which includes an L1 norm calculator block), and others.

Challenges

The main challenge with developing the architecture was maintaining the pipeline in the denoising path, from the DCT block to the Haar transform. This is due to the DCT transform being applied to each block on the group and the Haar to each position of all the blocks in a group. This means that to maintain the pipeline it is necessary to have two DCT blocks and consequently two IDCT blocks.

Next Tasks

Next week, work will be focused on finishing the system level architecture and starting the development of verilog code.

Bernardo Manuel Aguiar Silva Teixeira Cardoso