Weekly Report

Week 4: 09/03/2015 - 13/03/2015

Work Developed

The system level architecture was finished. It consists on an array of matching processors, each one processing a different image coordinate in parallel, and a denoising path (DCT, Haar, HT and Wiener, inv Haar, IDCT), that does the collaborative filtering for each group formed in the matching processors. There are also various memory modules as well as control finite state machines.

Challenges

The main challenge with developing the architecture was maintaining the pipeline in the denoising path, from the DCT block to the Haar transform. This is due to the DCT transform being applied to each block on the group and the Haar to each position of all the blocks in a group. This means that to maintain the pipeline it is necessary to have two DCT blocks and consequently two IDCT blocks.

Next Tasks

Next week, work will be focused on starting the development of verilog code for the matching processors.

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