Weekly Report

Week 5: 16/03/2015 - 20/03/2015

Work Developed

The implementation and simulation of the matching processor was completed in this week. A full correct behavior was verified between the verilog testbench and the MATLAB implementation, i.e., the processor "creates" the same groups as expected. The matching processor includes three modules: a memory to store the image neighborhood being processed, the l1 norm block that computes the distance between blocks, and a sorter block that chooses the sixteen minimum distances.

Challenges

The main challenge with developing the matching processor was ensuring that the sorter block only operates when correct distances are produced by the l1 norm block, which occurs when processing blocks in a different column.

Next Tasks

Next week, work will be focused on starting the development of verilog code for the denoising path.

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