Weekly Report

Week 6: 23/03/2015 - 27/03/2015

Work Developed

In this week, the denoising path implementation and simulation was completed. The results of the verilog testbench are on par with the MATLAB algorithm, with only some pixels being rounded to a different value with an offset of 1 (for example 161 instead of 160). This is believed to be due to the limited number of bits in the fixed point operations during the denoising pipeline, and this will be further investigated. The denoising path consists of a control module, the fifo that holds the positions of the group, a position decoder to access a memory that contains the part of the image being processed, and the denoising pipeline that is composed by the DCT and Haar transforms, the hard thresholding block, and the inverse Haar and IDCT.

Challenges

The main challenge with developing the denoising path was the control of the hard thresholding block, which produces a weight given by the number of non zero entries in each group. This way, the register holding this value must be cleared when processing a new group.

Next Tasks

Next week, work will be focused on development of verilog code for the memory interface and general control of the system.

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