Weekly Report

Week 12: 04/05/2015 - 08/05/2015

Work Developed

This week, progress with testing the system was done. The first error found was that the AXI reset signal was active low, which was not accounted for in the master control module, which meant the system was never starting. The second problem was related with the AXI Master operation. Reading from RAM to BRAM on the PL was working, but writing back to RAM had some issues. In order to try solving this problem, Mino's code was reviewed carefully, but as no problems were found, the AXI Master code was changed to the Xilinx IPIF code. Even with this changes, the memory interface wasn't working, so an AXI Slave approach was taken and will be tested on the following week.

Challenges

The main challenges this week were related with figuring out where the problems reside in the System, specially when a specific problem is being caused by multiple errors, which makes debugging a cumbersome process.

Next Tasks

Next week, work will be focused on continuing the testing of the system on the ZYNQ System on Chip, specifically the AXI Slave approach to the memory access.

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