Universidade do Porto
FEUP Faculdade de Engenharia

Doctoral Programme in Electrical and Computer Engineering at FEUP

Course Description

Course

Title	Language	Level	Term
Test and Design for Testability	English	PhD	2

Course coordinator

Name	Category	Institution
José Manuel Martins Ferreira	Associate Professor	FEUP

Other lecturers (not TA)	Institution
José Alberto Peixoto Machado da Silva Hélio de Sousa Mendonça	FEUP FEUP

Pre-requisites

1- Electronic circuits covering:
- Electronic devices
- Analysis of electronic circuits
- Digital circuits

2- Microprocessor based systems

Objectives

This course offers an up-to-date education on techniques and methodologies for testing and designing microelectronic circuits (both digital and mixed-signal) with embedded testability features. The curricular contents address mainly production testing issues, but characterization as well as maintenance tests will also be mentioned. Students are expected to acquire a thorough knowledge on IC and board testing, as well as on the approaches and tools commonly used to deal with testability issues.

Contents

The Test and Design for Testability contents was designed aiming to familiarize students with the most well known hierarchical and standard approaches to testing and designing for testability of electronic circuits, considering integrated printed-circuit boards, integrated circuits, and other monolithic substrate implementations.

The first module introduces the main issues which make testing a so critical stage in production manufacturing both in economic and technical terms, and provides an overview on defects and fault modelling, as well as on the foundations of test vector generation approaches.

These subjects are then developed more in detail in the second module which is devoted to studying design for testability techniques for digital circuits, starting with the generic scan design and structured boundary-scan standard approaches. Testability analysis and optimization methodologies at the register-transfer level are then studied as a means to attain enhanced testability solutions. The issue of designing safety critical digital systems is partially covered with the study of methodologies to design fault-tolerant systems implemented within field-programmable gate arrays.

The testing of memories is a domain which deserves a module of its own. In the third module memories' specific faults models and test generation algorithms are addressed concerning static and dynamic memories. A hands-on approach using the Advantest ATLWorks framework is favoured.

The fourth module addresses the testing analog and mixed-signal circuits' domain. The peculiarities of testing analog circuits, comparing to digital testing, are evaluated. The IEEE 1149.4 test infrastructure is described and illustrated with the support of JTAG Technologies' BST test program generation tools. Finally, design for testability and built-in self-test schemes of different analog and mixed-signal macros, comprising filters, A/D and D/A converters, phase-locked loops, are described relying on evaluating particular case studies.

Course delivery and assignments proposed to students were designed to promote a close interaction between theoretical contents and real-world applications.

Course Outline

Module I: Rationale and Testing Economics
1- Testing and test equipment
2- Test economics and product quality
3- Fault models, fault simulation and test vector generation

Module II: Digital design for testability
1- From scan design to boundary-scan testing
2- Digital extensions to the IEEE 1149.1 standard
3- Register-transfer level testability analysis and improvement
4- Fault-tolerant design within FPGAs

Module III: Memory testing
1- Memory architecture and defect trends
2- Fault modeling
3- Test pattern generation algorithms

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Module IV: Analog and mixed-signal design for testability
1- Digital x analog testing worlds
2- The IEEE1149.4 standard for a mixed-signal test bus
3- Structural and parametric testing in mixed-signal circuits
4- Built-In Self-Test of analog and mixed-signal circuits

Main Bibliography

Miron Abramovici, Melvin A. Breuer, Arthur D. Friedman, "Digital Systems Testing & Testable Design", W. H. Freeman & Company, 1990.

Michael L. Bushnell and Vishwani D. Agrawal, "Essentials of Electronic Testing for Digital, Memory & Mixed-Signal VLSI Circuits", Springer Science, 2000.

Mark Burns, Gordon Roberts, "An Introduction to Mixed-Signal IC Test and Measurement", Oxford University Press, 2001.

Software

JTAG Technologies' BST test program generation tools

CAD design tools (CADENCE)

Spice

Advantest ATLWorks

Teaching

This course comprises two lectures per week with practical/lab works. The lectures will be used for various types of presentations. The practical/lab component will be used for software training, experimenting with prototypes, and project development.

Assignments

A weekly individual homework assignment, with a designated set of exercises, and/or literature reading and simulation, will be appointed along the duration of the course. During the first two weeks, a set of review assignments will be appointed to help students to recall the necessary background. Each assignment is due at the end of the week that follows its presentation, and the full set of assignments will account for 30% of the final grade, including their presentation in the class.

A project will be assigned for each module, proposed for individual work or 2-element teams.

Module 1: Rationale and Testing Economics.

Module 2: Digital design for testability.

Module 3: Memory testing.

Module 4: Analog and mixed-signal design for testability.

An appropriate written report is expected from each project, to be delivered within one-week of its final date.

At end of the semester, the students will deliver a formal presentation of their project work. This component accounts for 30% of the final grade.

Grading policy

Student evaluation comprises the following components:
Assignments: A
Projects: P
Midterm Exam: ME
Final Exam: FE

The final score will be calculated according to the following rule:
30%×A+30%×P+20%×ME+20%×FE

Grading will be either PASS or FAIL.

A Passing grade corresponds to a minimum of 2/3 of the maximum score.

Evaluation procedure for students under special legal provisions

All evaluation procedures of regular students apply in this case as well, i.e., assignments, project work and exams. However, all students under special legal provisions *may* be exempt to attend regular classes and deliver their assignments in the same dates as regular students.

Improving grades

Not applicable in a PASS/FAIL policy.