2nd Workshop on Design Tools and Architectures for Multi-Core Embedded Computing Platforms (DITAM'2013)

Berlin, Germany, January 22, 2013, Website: http://www.fe.up.pt/ditam2013

To be held in conjunction with:

the 8th International Conference on High-Performance and Embedded Architectures and Compilers (HiPEAC)
January 21-23, 2013, Berlin, Germany.

Location: Radisson Blu Hotel in the center of Berlin
(http://www.radissonblu.com/hotel-berlin)

Contents

ORGANIZATION

General Co-Chairs:

- João M. P. Cardoso, Universidade do Porto, Portugal, jmpc@acm.org
- Michael Huebner, Ruhr-Universität Bochum, Germany, Michael.Huebner@ruhr-uni-bochum.de

Run-time Adaptivity Techniques Session Chair:

- Cristina Silvano, Politecnico di Milano, Italy

Heterogeneous Many-Core Architectures Session Chair:

- Stephan Wong, TUDelft, The Netherlands

Design Tools and Methodologies Session Chair:

- Zlatko Petrov, Honeywell, Czech Republic

Web Submissions and Poster/Demos Session Chairs:

- Vittorio Zaccaria, Politecnico di Milano, Italy
- Diana Goehringer, KIT, Germany

Panel Session Chair:

- Michael Huebner, Ruhr-Universität Bochum, Germany

TARGET AUDIENCE

The workshop tries to bring together researchers actively working on methodologies, design tools, and architectures, for multi-core embedded computing platforms.

TOPIC AREAS

The workshop has three main sessions:

- **Heterogeneous Many-Core Architectures:** on the most relevant problems arising during the design exploration and optimization of heterogeneous many/multi core architectures.
- **Design Tools and Methodologies:** on the state-of-the-art of tool development and on fresh ideas to make design tools aware of non-functional requirements and different target architectures.
- **Run-time Adaptivity Techniques:** on the state-of-the-art techniques to dynamically manage and adapt the resources of the target architecture to runtime workloads and/or new applications.

OVERVIEW

Embedded computing is one of the computing areas where multi/many-core architectures are being used to achieve high-performance and/or energy savings. Tight and demanding requirements, short time-to-market and possible product upgrades, make the development of applications and the design of embedded architectures very challenging. Techniques for hardware/software co-design, for configuring the system according to application needs, for programming the multiple cores, and for generating customized hardware accelerators are currently hot topics of research. Furthermore, customization via reconfigurable hardware, run-time resource management, and run-time adaptability are seen as promising techniques to adapt the embedded computing architecture to the application requirements.

This workshop serves as a privileged forum to discuss recent research and development advances from academia and industry.

This workshop is mainly organized around the final results of three EU funded FP7 projects, namely **2PARMA** (*PARallel PAradigms and Run-time MAnagement techniques for Many-core Architectures*, http://www.2parma.eu/), **ERA** (*Embedded Reconfigurable Architecture*, http://www.era-project.eu/), and **REFLECT** (*Rendering FPGAs to Multi-Core Embedded Computing*, http://www.reflect-project.eu/). We plan to have contributions from other ongoing EU funded FP7 projects.

This workshop presents the approaches and research efforts being explored, the results achieved, and the proposed research avenues of those projects.

Furthermore, we have four invited talks given by prestigious speakers. These invited talks will possibly give other views not necessarily tied to the specific objectives of the projects. Finally, a panel will allow a fruitful discussion between members from academia and from industry.

FINAL PROGRAM

10:00	**10:10**	**Opening Session by General Co-Chairs: João M. P. Cardoso**, Universidade do Porto, and **Michael Huebner**, Ruhr-Universität Bochum
10:10	**10:20**	**Introduction to Poster/Demo Sessions: Vittorio Zaccaria** , Politecnico di Milano, Italy, **Diana Goehringer**, KIT, Germany
10:20	**12:00**	**Design Tools and Methodologies Session - Organizer: Zlatko Petrov, Honeywell, Czech Republic**
10:20	10:50	**Wayne Luk, Machine Learning for Reconfigurable Design**, Imperial College London, UK
10:50	***11:30***	***Posters/Demos Session - COFFEE BREAK, Organizers: Vittorio Zaccaria , Politecnico di Milano, Italy, Diana Goehringer, KIT, Germany***
11:30	12:00	**Zlatko Petrov, REFLECT: Final Achievements and Results, Honeywell, Czech Republic**
12:00	**13:00**	**Panel on: "Embedded Multi-core Computing: Challenges and Trends"** **Panel Organizer and Moderator:** Michael Huebner, Ruhr-Universität Bochum, Germany **Panel Members: Arnon Friedmann** (Texas Instruments, USA), **Ronald P. Luijten** (IBM Zurich Research Laboratory, Switzerland), **William Fornaciari** (Politecnico di Milano, Italy), and **David Bernstein** (IBM Haifa Research Lab,Israel).
13:00	***14:00***	***Lunch***
14:00	**15:30**	**Run-time Adaptivity Techniques Session - Organizer: Cristina Silvano, Politecnico di Milano, Italy**
14:00	14:30	**Marco Platzner**, ***The Role of Heterogeneous Multi-cores in Self-aware Computing Systems***, University of Paderborn, Paderborn, Germany
14:30	15:00	**Cristina Silvano**, ***2PARMA: Final Achievements and Results***, Politecnico di Milano, Milan, Italy
15:00	15:30	**Jürgen Teich, Safe(r) Loop Computations on Multi-Cores, FAU Erlangen, Germany**
15:30	***16:30***	***Posters/Demos Session - COFFEE BREAK, Organizers: Vittorio Zaccaria , Politecnico di Milano, Italy, Diana Goehringer, KIT, Germany***
16:30	**18:00**	**Heterogeneous Many-Core Architectures Session – Organizer: Stephan Wong, TUDelft, Delft, The Netherlands**
16:30	17:00	**Ronald P. Luijten**, ***The DOME Embedded 64-bit Microserver Project***, IBM Zurich Research Laboratory, Zurich, Switzerland
17:00	17:30	**Stephan Wong**, ***ERA: Final Achievements and Results***, TUDelft, Delft, The Netherlands
17:30	18:00	**Alex Ramirez**, ***Explicit memory hierarchy management in the ENCORE architecture***, Universitat Politècnica de Catalunya and Barcelona Supercomputing Center, Barcelona, Spain
18:00	**18:10**	**Final Wrap up**

Machine Learning for Reconfigurable Design

Wayne Luk, Imperial College London, UK

Abstract

This talk provides an overview of research relating machine learning and reconfigurable computing. Two themes are covered. The first theme concerns how machine learning can benefit reconfigurable computing, for example by speeding up design space exploration in developing reconfiguration computing systems. The second theme concerns how reconfigurable computing can benefit machine learning, for example by accelerating key applications. The potential of further development relating machine learning and reconfigurable computing will also be presented.

REFLECT: Final Achievements and Results

Zlatko Petrov, Honeywell, Czech Republic

Abstract

REFLECT, standing for Rendering FPGAs to Multi-core Embedded Computing, is a 3-year programme co-funded by the European Commission, out of the ICT budget. The total project cost is €3.7M. The project started on Jan 1st 2010 and finished on Dec 31st 2012. The consortium is consisting of eight partners from five EU countries. Project coordinator is Zlatko Petrov (Honeywell International) and project scientific coordinators are João M.P. Cardoso (Faculty of Engineering of the University of Porto) and Pedro C. Diniz (Institute for Systems and Computer Engineering, Research and Development in Lisbon).

The REFLECT project developed, validated and evaluated a novel compilation and synthesis system approach that relies on Aspect-Oriented Specifications to convey critical domain knowledge to all development steps, and to help designers to develop efficient FPGA-based heterogeneous multi-core computing systems. Our research and development agenda aimed at developing a new foundation combining distinct, but synergistic, areas of research: *aspect-oriented specifications*, *hardware compilation*, *design patterns and hardware templates*. Overall, this project was aiming at:

- Making the reconfigurable technology acceptable for avionics and audio/video domains:
  - Lowering barrier of adoption of technology;
  - Enable system portability to new architectures;
- Improving productivity
  - Accelerating design cycles by more than two orders of magnitude;
  - Allow user to have full control of design flow stages;
  - Control design & mapping in a consistent, systematic and verifiable way.

The REFLECT consortium evaluated the effectiveness of its approach with applications from the domains of audio/video processing and real-time avionics. Four applications have been selected, namely: MPEG audio encoding - it represents the ISO reference code for Layer 3 MPEG-2 encoding; G.729 - an audio data compression algorithm for voice that compresses digital packets of 10 ms duration; 3D path planning – it computes a path between the current and goal vehicle positions integrated as part of modern unmanned aerial vehicles (UAVs),

Stereo navigation – it is intended for airplane localization in case a GNSS (Global Navigation Satellite System) is temporarily unavailable and the plane has to localize itself for a period of time.

This presentation will describe the technical approach of the REFLECT project, major achievements and finally major outcomes of the evaluation process conducted by the industrial partners within the REFLECT consortium.

The Role of Heterogeneous Multi-cores in Self-aware Computing Systems

Marco Platzner, University of Paderborn, Paderborn, Germany

Abstract

In this talk we first give an overview over EPiCS, an ongoing FP7 FET project that aims at laying the foundation for engineering the novel class of proprioceptive computing systems. Proprioceptive computing systems collect and maintain information about their state and progress, which enables self-awareness by reasoning about their behaviour, and self-expression by effectively and autonomously adapting their behaviour to changing conditions. Then we show that concepts of self-awareness and self-expression are also applicable at the level of heterogeneous compute nodes. Heterogeneous compute nodes integrate processor cores, reconfigurable hardware cores, fixed-function cores, memories and interconnects and are of increasing importance. However, there still is a lack of efficient programming models. We present ReconOS, an architecture and programming environment that extends the widely-used multithreading programming model across the software/hardware boundary and thus facilitates the creation of self-aware computing systems.

2PARMA: Final Achievements and Results

Cristina Silvano, Politecnico di Milano, Milan, Italy

Abstract

The 2PARMA (PARALLEL PARADIGMS AND RUN-TIME MANAGEMENT TECHNIQUES FOR MANY-CORE ARCHITECTURES) project (Jan. 2010-Dec. 2012) tackles the issue of programmability of multi-core computing fabrics at both programming language and operating system level.
The project focuses on the definition of a compilation tool chain supporting a parallel programming model combining component-based and single instruction multiple-thread (OpenCL) approaches. The project also provides a run-time resource management framework (BBQ) driven by design space exploration to automatically generate energy-delay operating points for multiple applications running on many-core computing fabrics.
The 2PARMA project demonstrate methodologies, techniques and tools by using innovative hardware platforms provided and developed by STMicroelectronics (P2012 STHORM) and IMEC (COBRA Platform).
To ensure a wide range of application scenarios comprising the typical computation-intensive workload of a general-purpose computing system, a set of industrial high performance demanding applications have been used and customized by using the techniques and methodologies developed in 2PARMA project. Applications' architecture, development and integration leverage from the acknowledged experience of three partners from the

Consortium: Fraunhofer HHI for scalable video coding application, RWTH Aachen University for cognitive radio (MAC and physical layer), and IMEC for multi view image processing.

Safe(r) Loop Computations on Multi-Cores

Jürgen Teich, FAU Erlangen, Erlangen, Germany

Abstract

The necessity of satisfaction of non-functional constraints such as guaranteed data processing throughput, deadline reactive processing or safety properties is of utmost importance for the successful introduction of multi-core technology in many future embedded system products.

In this talk, we consider the joint conceptualization of architecture, methods and tools that allow a developer to specify a certain safety level for a quite general and important class of loop computations. Loop programs are known to be quite amenable to parallel processing and are typically also quite scalable. However, no existing work is known to us how to make loop computations safe so to guarantee the correctness of the corresponding computed results of a loop program at run-time.

In this realm, we propose first ideas how, dependent on a specified "safety level", the core allocation might be properly controlled for allowing concepts such as DMR and TMR known for standard processor systems to loop computations on multi-cores including the way how determistic voting may be efficiently implemented on a class of domain-specific multi-core architectures called "tightly-coupled processor arrays" (TCPAs).

We conclude how these concepts of redundant in-sync loop computation might be nicely supported by the recent parallel computing initiative called invasive computing.

The DOME Embedded 64-bit Microserver Project

Ronald P. Luijten, IBM Zurich Research Laboratory, Zurich, Switzerland

Abstract

IBM research – Zurich and Astron recently started the 5 year DOME research project, co-funded by the Dutch government, to develop technology roadmaps to build the SKA (Square Kilometer Array) radioastronomy antenna. The DOME microserver demonstrator addresses high density, low- cost and low-power computing requirements in the SKA project. The microserver demonstrator also targets IBMs anticipated business needs. In this presentation, I will outline the microserver objectives, requirements and show what we are currently building using one of the latest Freescale 64 bit PPC parts. I will furthermore show which 3 key applications we can already run on this platform.

ERA: Final Achievements and Results

Stephan Wong, Delft University of Technology, Delft, The Netherlands

Abstract

ERA (Embedded Reconfigurable Architectures) is a 3-year project funded by the EU under the FP7 framework programme (starting January 2010) with the following partners: (1) Delft

University of Technology (NL) - coordinator, (2) Industrial Systems Institute (GR), (3) Universita' degli Studi di Siena (IT), (4) Chalmers University (SE), (5) University of Edinburgh (UK), (6) Evidence (IT), (7) ST Micro (IT), (8) IBM (IL), (9) Universidade do Rio Grande do Sul (BR), and (10) Uppsala University (SE). The ERA project addresses issues rising from a scenario in which the complexity and diversity of embedded systems is rising and causing extra pressure in the demand for performance at the lowest possible power budget and in which designers face the challenges brought by the power and memory walls in the production of embedded platforms.

The focus of the ERA project is to investigate and propose new methodologies in both tools and hardware design to break through these walls and help design the next-generation embedded systems platforms. The proposed strategy is to utilize adaptive hardware to provide the highest possible performance with limited power budgets. The envisioned adaptive platform employs a structured design approach that allows integration of varying computing elements, networking elements, and memory elements. More precisely, we focused on the dynamic adaptation of our platform (of the computing, networking and memory elements) to the software requirements and the operating environment targeting performance, power/energy, and resource availability.

Key achievements are:

- development of a reconfigurable parameterized (softcore) processor that is capable of dynamically adjusting its issue width and other parameters (register file size, type and number of functional units, and memory bandwidth).
- definition of dynamically adjustable memory hierarchies (caches) and their mechanisms that are capable of on-the-fly (smooth) adaptation to application behavior in cache size, cache line size, and set associativity.
- development of a dynamically reconfigurable network-on-chip (NoC) that can adjust itself to the traffic flowing through its nodes.
- characterization of embedded applications (working on top of an embedded OS) in how to best map application characteristics to the parameters of the earlier mentioned hardware components.
- definition of new compilation techniques to deal with the underlying dynamic behavior of the hardware components.
- extension of an embedded OS to manage the hardware components and to schedule a given set of applications that need to be executed.

Several key deliverables are:

- three working hardware platforms with the following characteristics: (1) an OS capable of controlling the reconfigurable parameterized processors, (2) the developed reconfigurable processor with its own memory hierarchy, and (3) an NoC incorporating several of the developed reconfigurable processors.
- a cycle-accurate simulator in which the cores, memory hierarchy, and NoC can be simulated incorporating many reconfiguration techniques developed within the ERA project.
- two independent toolchains that allow one to code C and arrive at executables that can be executed on the hardware platforms and the simulator. One toolchain is based on the closed-source HP compiler and the other is based on GCC.

This presentation will describe the technical approach of the ERA project, major achievements, and the final ERA platform developed within the ERA project. This platform is made available under an academic license and is accompanied with an extensive tutorial.

Explicit memory hierarchy management in the ENCORE architecture

Alex Ramirez, Universitat Politècnica de Catalunya, Barcelona Supercomputing Center (BSC), Barcelona, Spain

Abstract

The contents of the cache hierarchy is determined by the replacement policy, and the hardware prefetcher, often leading to sub-optimal decisions, performance degradation, and low scalability. In the ENCORE architecture we provide the user with block directives to explicitly manage the cache hierarchy, enabling fetching and flushing of data in parallel with the computation. Furthermore, we have extended the NANOS++ runtime system to automatically generate such directives for OmpSs applications, and manage the caches transparently from the user, and better than the hardware.

PANEL

Panel on: **"Embedded Multi-core Computing: Challenges and Trends"**

Panel Organizer and Moderator: **Michael Huebner**, Ruhr-Universität Bochum, Germany

Panel Members:

- **Arnon Friedmann** (Texas Instruments, USA)
- **Ronald P. Luijten** (IBM Zurich Research Laboratory, Switzerland)
- **William Fornaciari** (Politecnico di Milano, Italy)
- **David Bernstein** (IBM Haifa Research Lab, Israel)

POSTERS/DEMOS SESSIONS

Below are the posters accepted for presentation (posters are available at ***http://www.fe.up.pt/ditam2013***).

In addition, demos and posters about the three FP7 Projects, 2PARMA, ERA, and REFLECT, will be presented during the two posters/demos sessions.

Authors and Affiliations	Title
Luigi Pomante, University of L'Aquila – DEWS, Italy	System-Level Design Space Exploration for Dedicated Heterogeneous Multi-Processor Systems
Jens Brandenburg, and **Benno Stabernack**, Fraunhofer Institut für Nachrichtentechnik, Germany	Performance and Memory Access Analysis for Embedded Multi-Core Media Signal Processing Platforms using NoCTrace
Simon Barner[1], **Jia Huang**[1], **Andreas Raabe**[1], and **Alois Knoll**[2], [1]Fortiss GmbH, Germany, and [2]Institut für Informatik VI, [2]Technische Universität München, Germany	A Framework for Embedded System Design for MPSoCs
Thales Taborda, **Gabriel Nazar**, and **Luigi Carro**, UFRGS - Universidade Federal do Rio Grande do Sul, Brazil	Evaluating the Weighted Fault Sensitivity of the Components of a VLIW Architecture
Paulo Santos[1], **Gabriel Nazar**[1], **Fakhar Anjam**[2], **Stephan Wong**[2], **Debora Matos**[1], and **Luigi Carro**[1], [1]UFRGS - Universidade Federal do Rio Grande do Sul, Brazil, [2]Delft University of Technology, The Netherlands	A Fully Dynamic Reconfigurable NoC-based MPSoC: The Advantages of a Multi-Level Reconfiguration
Laszlo Bako[1], **Sandor-Tihamer Brassai**[1], **Lajos Losonczi**[2], and **Laszlo-Ferenc Marton**[1], [1]Sapientia - Hungarian University of Transilvania, Electrical Enginnering Department, Targu-Mures, Romania, [2]Lambda Communications Ltd., Romania	Multiple processor core systems on FPGA circuits implementing bio-inspired neural networks for classification tasks
Mateus Rutzig[1], **Antonio Carlos Schneider**[2], and **Luigi Carro**[2], [1]Federal University of Santa Maria, Brazil, [2]UFRGS - Universidade Federal do Rio Grande do Sul, Brazil	CReAMS: An Embedded System Platform
Sandor-Tihamer Brassai[1], **Laszlo Bako**[1], **Lajos Losonczi**[2], and **Laszlo-Ferenc Marton**[1], [1]Sapientia - Hungarian University of Transilvania, Electrical Engineering Department, Targu-Mures, Romania, [2]Lambda Communications Ltd., Romania	Parallel pipeline solution for hardware implementation of artificial neural networks with in circuit real time weight update
Rabie Ben Atitallah, LAMIH, University of Valenciennes/ INRIA-Lille Nord Europe, France	Heterogeneous CPU/FPGA computing system for avionic test applications