

# System-Level Design Space Exploration for Dedicated Heterogeneous Multi-Processor Systems

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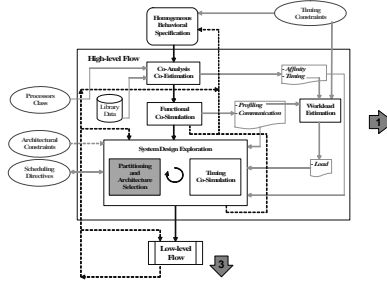
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## Overview

- This project addresses the problem of the co-design of Dedicated Heterogeneous Multi-Processor Systems
- In particular, the presented work starts from an existing co-design flow with the aim to propose innovative extensions to the system design exploration task
- Such extensions allow the methodology to propose an HW/SW partitioning of the specification, mapping the partitioned entities onto an automatically selected heterogeneous architecture, being aware of both the computational and communication components
  - Automatic selection of the heterogeneous processors composing the platform
  - Automatic selection of the links and the topology interconnecting the selected processors

Follow the navigation tips! →

## The System-Level Co-Design Flow



## The System-Level Co-Design Flow

- The entry point is a behavioral description of the application
- The first step (Co-Analysis&Co-Estimation) extracts some important data about the system
  - The affinity of each functionality toward the considered processing elements and a set of estimations of the time required for the execution of each single operation
- Then, the specifications are simulated to verify correctness with respect to typical input data sets, extracting data characterizing the dynamic behavior of the system
  - Profiling and Communication Bandwidth
- Combining the data provided by the first step with the timing constraints allows the estimation of the load associated with each functionality
  - The analysis of such data is useful to evaluate the number of processors and the level of load balancing
- Two iterative steps constitute the System Design Exploration task
  - Partitioning and Architecture Selection, and Timing Co-Simulation

## Architectural Elements & Metrics

For each possible interconnection link it is considered a set of features

-Max bandwidth offered by the IL

-Min and max number of BBB that can use a single IL instance

-Relative cost (€)

-Feasibility constraints

### Saturation Index

$$I_s = 1 - \sum_{j=1}^m \frac{b_{ij} \cdot a_{ij}}{m}$$

### Exploitation Index

$$I_e = 1 - \sum_{j=1}^m \frac{c_j}{m}$$

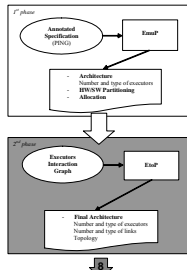
### Total Cost

$$I_c = \frac{\sum_{i=1}^m C_i}{m \cdot C_{max}}$$

### Cost Function

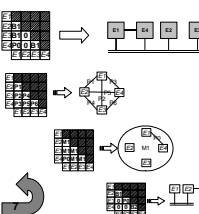
$$CF = w_s \cdot I_s + w_e \cdot I_e + w_c \cdot I_c$$

## Partitioning&Architecture Selection Step



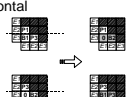
## Individuals & Cross-Over

### Possible Individuals



### Cross Over

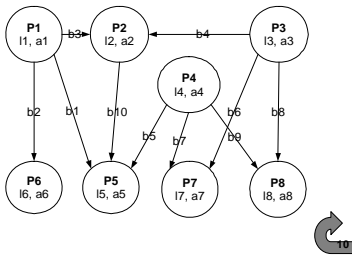
#### - Horizontal



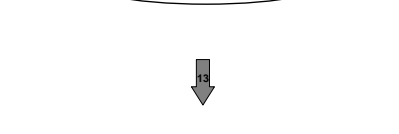
#### - Vertical



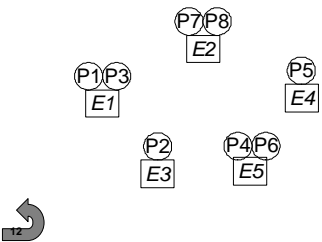
## Example: Step 1 Annotated Specification (CSP)



## Example

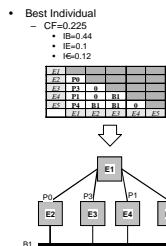


## Example: Step 2 Executors/Allocation View

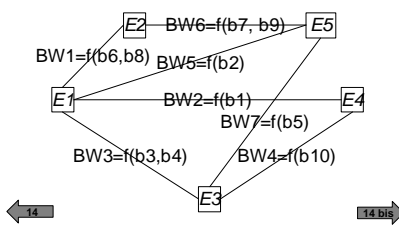


## Example: Step4 Results

- EIG
  - BW1=250
  - BW2=200
  - BW3=200
  - BW4=150
  - BW5=250
  - BW6=50
  - BW7=50
- Links Characterization
  - max bandwidth, max number of executors, relative cost:
  - P=(500, 2, 1)
  - B=(200, 8, 5)
  - M=(200, 80, 5)
- CF weights
  - WB=WE=0.35
  - WC=0.3



## Example: Step3 Executors Interaction Graph



## Example: Step4 bis Results

- EIG
  - BW1=250
  - BW2=200
  - BW3=200
  - BW4=150
  - BW5=250
  - BW6=50
  - BW7=50
- Links Characterization
  - max bandwidth, max number of executors, relative cost:
  - P=(500, 2, 4)
  - B=(250, 8, 2)
  - M=(200, 80, 5)
- CF weights
  - WB=WE=0.35
  - WC=0.3

