EVALUATING THE WEIGHTED FAULT SENSITIVITY OF THE COMPONENTS OF A VLIW ARCHITECTURE

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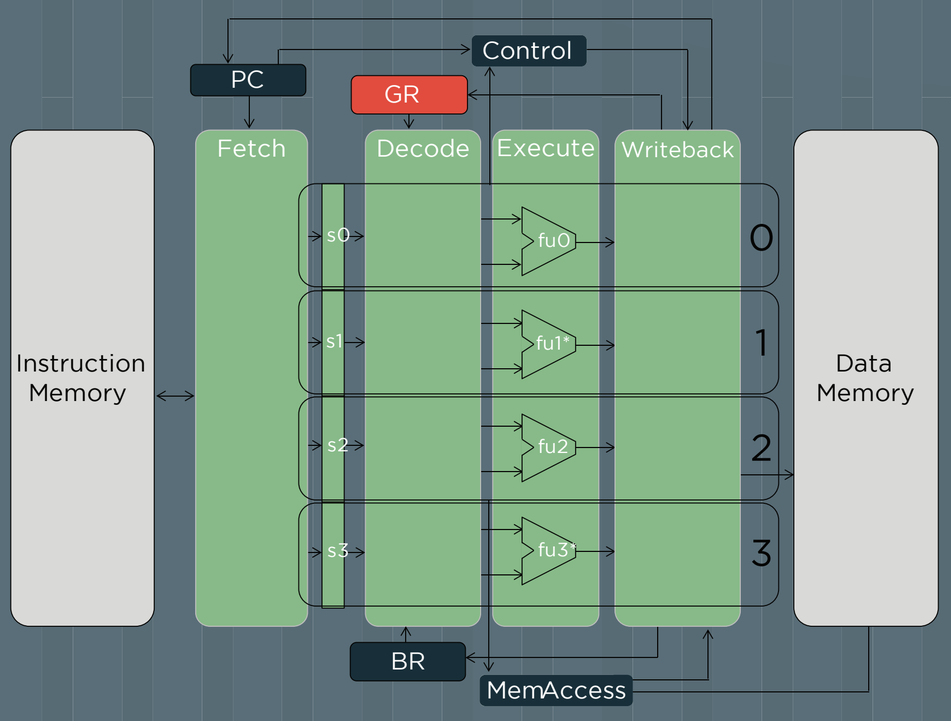
1. MOTIVATION:

- Very Long Instruction Word (VLIW) processors take advantage of the Instruction Level Parallelism to increase performance at a low cost of power.
- The energy efficiency of these processors makes them an attractive solution for embedded systems.
- Technology scaling, however, makes devices susceptible to Single Event Effects (SEEs), which must be counteracted in order to maintain an acceptable dependability.
- Achieving resilience to hardware faults is crucial to enable the use of VLIW processors on critical systems, where the high performance and low power provided by these architectures are important features, but high dependability remains a stringent constraint which must be satisfied with minimum cost and efforts.

2. METHODOLOGY:

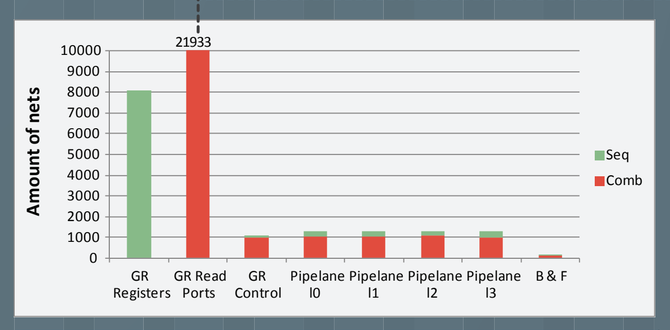
- In this work we have conducted a series of fault injection experiments on a VLIW processor (ρ-Vex), executing a 10x10 matrix multiplication, to determine what are the critical spots of this architecture, i.e., the ones that are more susceptible to lead to a functional failure when subject to transient faults.
- The experiments, which considered both the effects of SEUs and SETs, were executed on an FPGA to accelerate the process and to allow a large amount of faults to be injected in a timely manner.
- We measured the weighted sensitivity of the different components of the ρ-VEX processor to identify their contribution to overall sensitivity. This metric takes into account estimations of both the area and the fault propagation probabilities of each component. We have injected faults on each of the pipeline lanes, as well as in the register file and control signals.



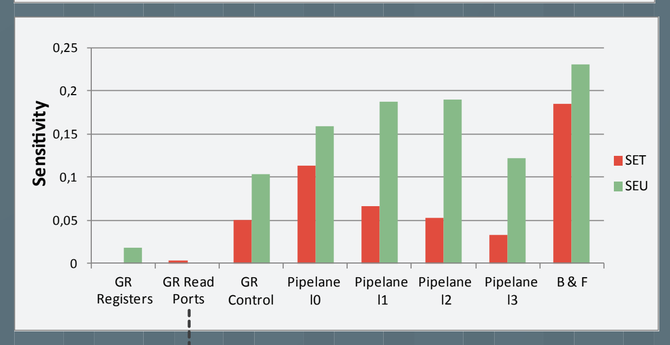
The ρ-Vex is a configurable and extensible VLIW processor, based on the VEX ISA, that supports multiple issue widths. We have used the 4-issue version of this architecture

3. RESULTS

- Each component presents different area occupation (approximated here by the amount of nets), but also very different fault sensitivities

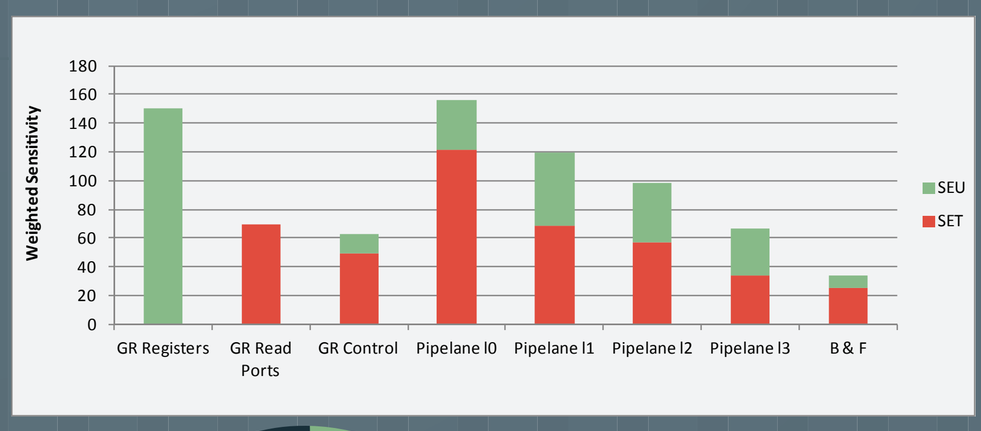


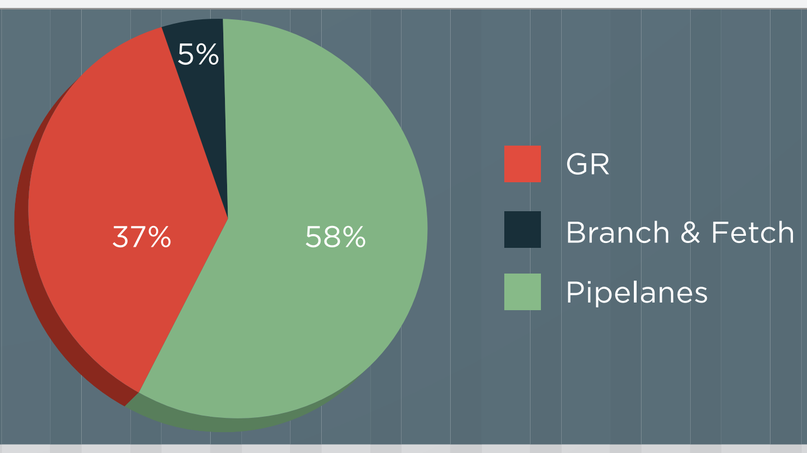
The GR Read Ports account for 80% of the nets of the processor.



But it is an area with very low sensitivity, due to its high masking probability.

- The weighted sensitivity (area sensitivity) shows the contribution of each evaluated component





4. CONCLUSIONS AND FUTURE WORKS

- Both area and functional properties (fault sensitivity) must be taken into account to estimate the contribution of each component to overall reliability.
- All evaluated components have a significant contribution to fault sensitivity and should be taken into account by fault injection experiments. In particular, the control circuitry has a small area but a high sensitivity, increasing its importance. Furthermore, it is the least redundant resource, increasing the complexity of providing fault tolerance to it.
- Future works include evaluating the impact of different benchmark applications on the sensitivity of each component, as well as evaluating the effectiveness of fault tolerance mechanisms using the developed tools.

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