A Fully Dynamic Reconfigurable NoC-based MPSoC:
The Advantages of a Multi-Level Reconfiguration

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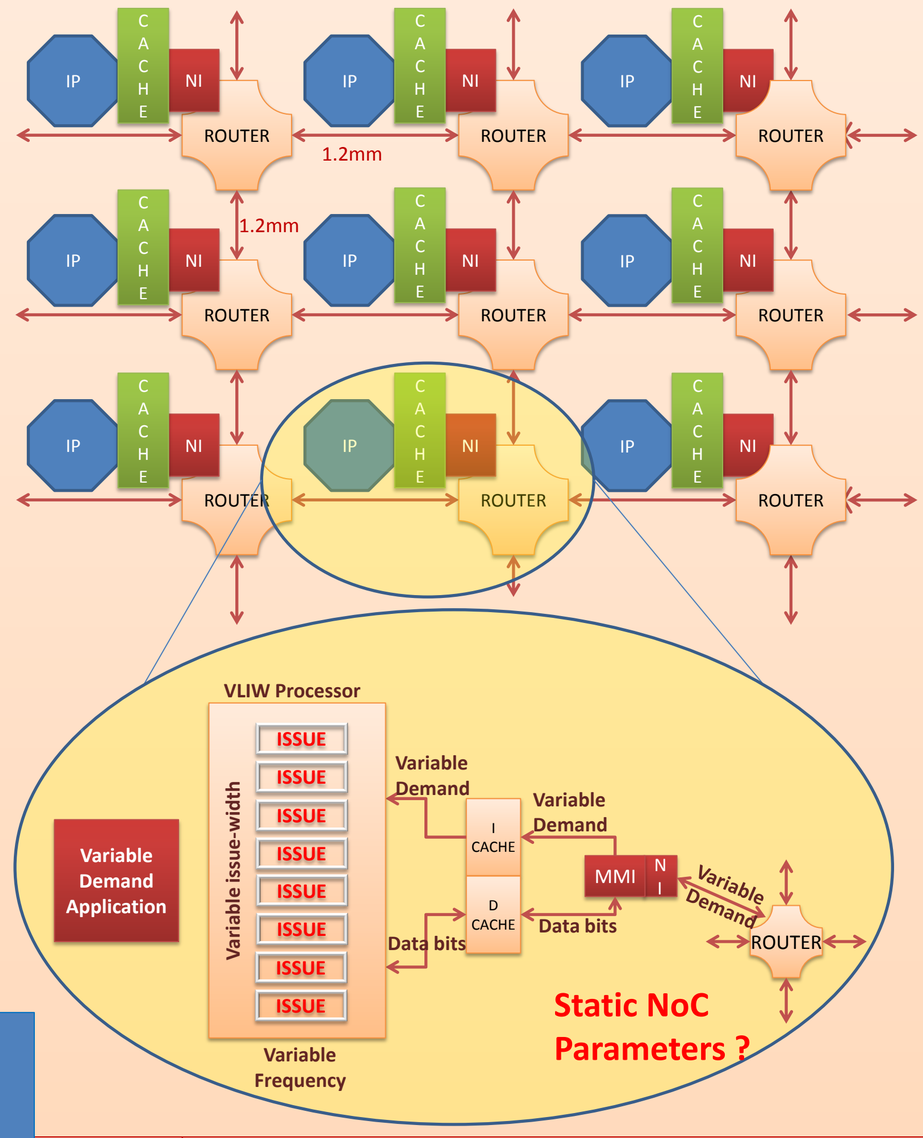
Introduction

Multiprocessors System on Chip (MPSoCs) have emerged as a technology trend to provide the needs for growing performance and integration of different features in a single integrated circuit. In these platforms, Networks-on-Chip (NoCs) have been adopted, providing reusability, scalability, parallelism and high bandwidth data communication.

However, the search in the design space is not only about performance, but also about consuming less power and energy. The increasing power density found in the newer manufacturing technologies makes it unfeasible for a system to operate at maximum performance the entire time. Thus, techniques able to significantly reduce the power consumption are essential for enabling the efficient use of aggressively scaled technologies.



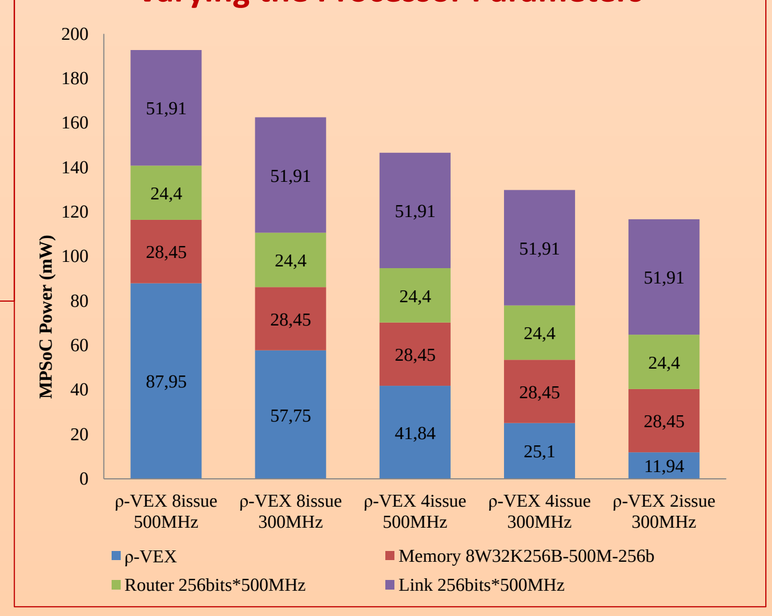
Goals

- Reducing power consumption without performance penalty for the system
- Optimal use of all components (processor, memory and communication)
- Identifying the optimum NoC configuration parameters for varying processor demand
  - Focusing on the instruction cache demand
- Taking into account:
  - Variable flit width
  - Variable operating frequency

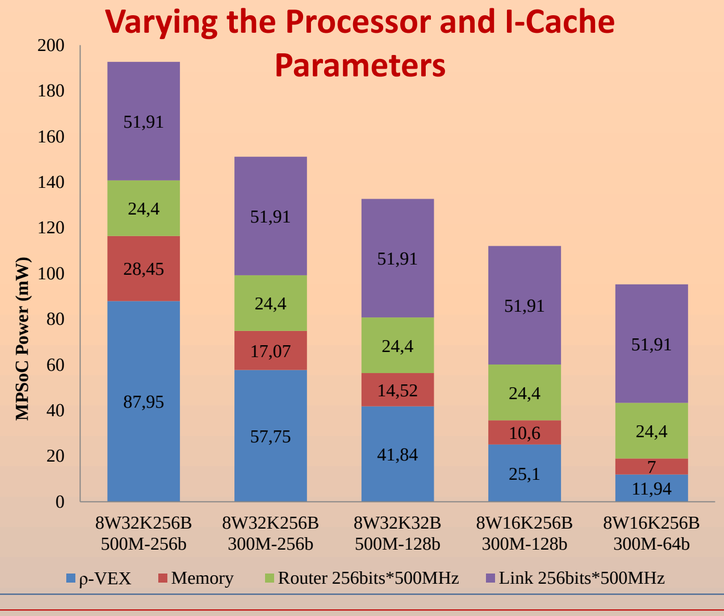
- The power and area were estimated with RTL Compiler and CACTI, both using a 65nm technology.
- The wires connecting the routers were estimated at 1.2mm, according to the extracted areas.

Varying the Processor Parameters

- **The issue-width of a VLIW processor can be reconfigured at run time by temporarily enabling or disabling functional units (FUs), thus reducing the power consumed by the processor.**
- The processor initially represented 45.6% of the power consumed by the MPSoC, being this value only 10.2% when reconfigured for ρ-VEX 2 issue 300MHz.
- Even when the processor power consumption is reduced 7.37 times, the entire system power is only reduced 39.45%.



Varying the Processor and I-Cache Parameters

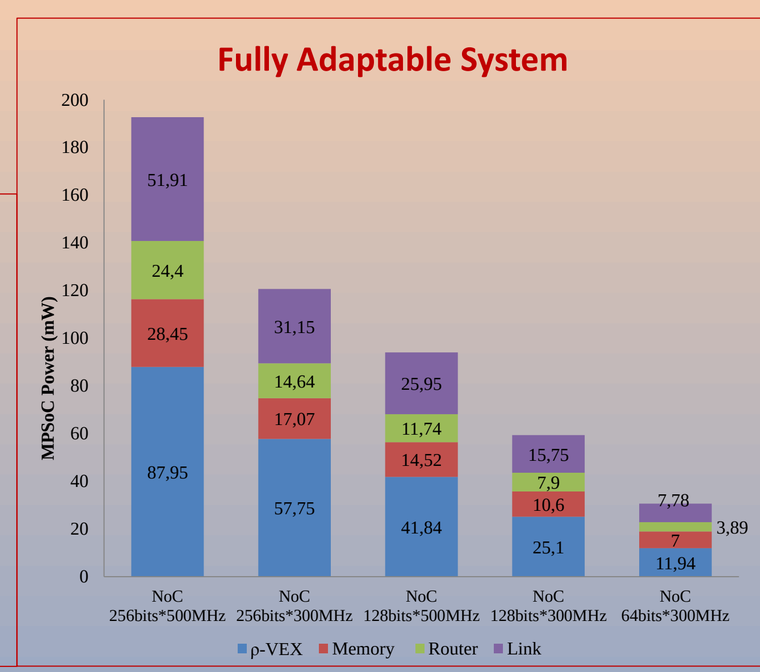


Varying the Processor and I-Cache Parameters

- **The configuration of the issue-width of the VLIW processor causes reduction of throughput required from the instruction cache memory, thus the correct reconfiguration of the cache can minimize the unnecessary power consumption.**
- When the power of the processor is reduced 7.37 times and the memory power is reduced 4.06 times, the overall reduction is limited to 50.58%, due to the NoC static nature.

Fully Adaptable System

- **In the experiment the frequency and flit-width of the NoC were reconfigured keeping the throughput required by the application.**
- By varying the frequency and data width of the router, its power consumption varies, as well as that of the router wires. By varying the data width of the NoC, there is also the possibility of powering off the buffers associated with the unused channel bits, leading to significant reductions in the total NoC power.
- When all elements are adapted to maintain compatible capabilities, the maximum power reductions are achievable. The total power reduction attainable by such a system is 84.12%, as there is no static component to limit the gains.



Conclusion and Future Works

We have presented and quantified the need for adaptability in all components that contribute significantly to system power consumption. Whenever there is a processor able to dynamically modify its processing capabilities and/or a memory with adaptable bandwidth, the optimal NoC configuration able to supply the system needs with minimal power will also change. Thus, leaving any of the system components with exceeding power or insufficient performance will make such a component either a source of energy waste or performance bottleneck.

Quantization of these gains is crucial to guide future research directions. For example, to consider heuristics to coordinate the optimum system configuration, taking into account all relevant layers at once, may successfully exploit the parameters presented. Furthermore, other reconfiguration directions, such as NoC routing algorithms or the processors register file size may be added to the design space exploration.

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