CReAMS: An Embedded System Platform

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Motivation

Embedded Devices

Shorter Lifetime

Run heterogeneous applications

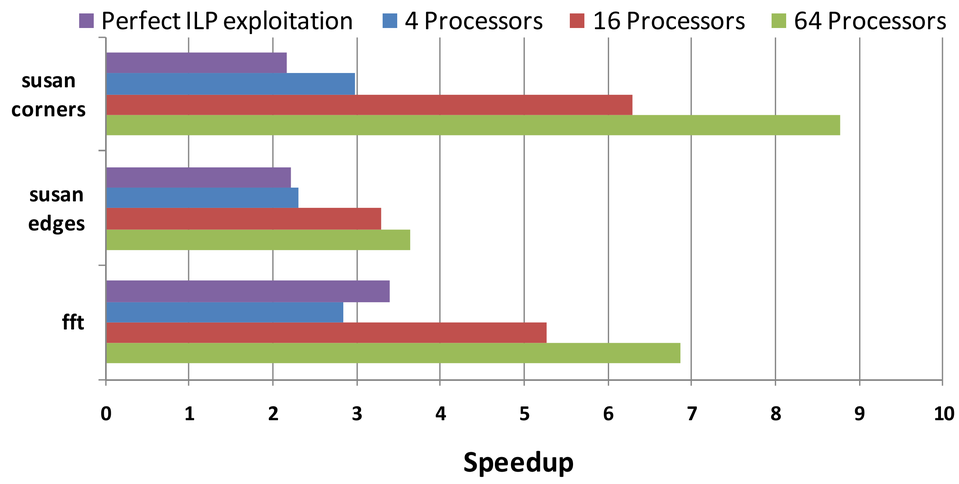
Current Platform Strategy

Dedicated accelerators (ASICs)

✚ Performance	▬ Execution of unforeseen applications
✚ Energy	▬ Many versions of platforms and tool chains
✚ Area	▬ Heterogeneous ISA
	▬ Software development process

What should be explored: ILP or TLP?

Mixed exploitation is mandatory



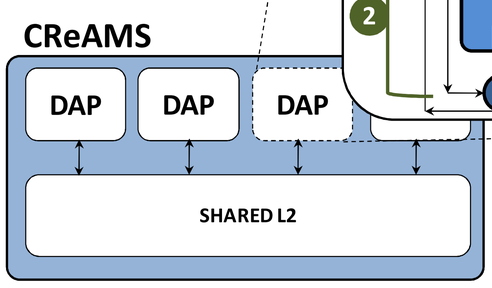
CReAMS

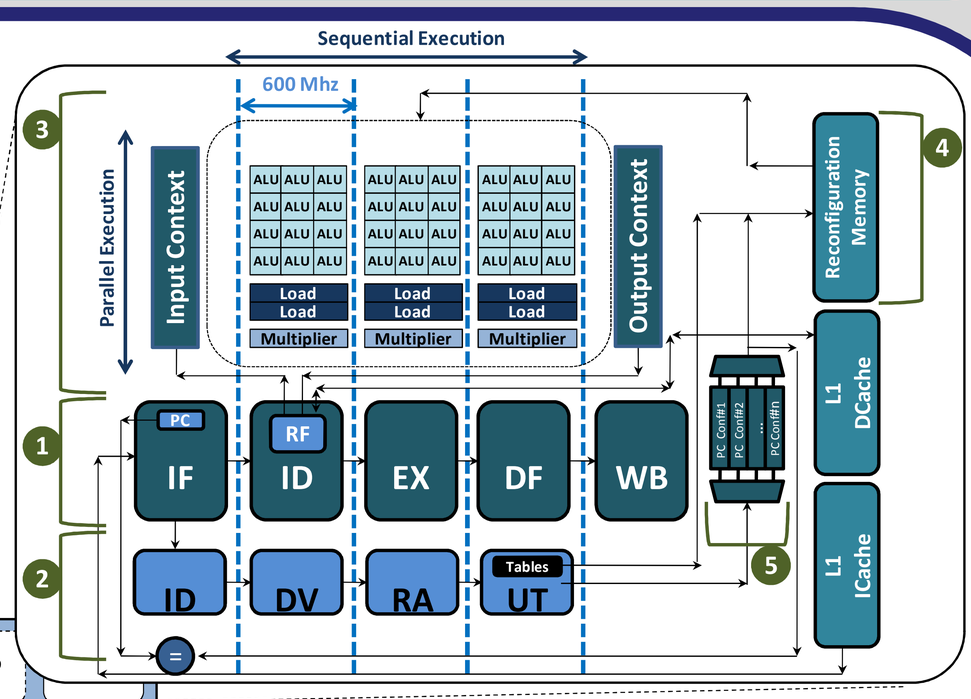
TLP exploitation

- **Multiple Dynamic Adaptive Processors (DAPs)**
  - Thread level parallelism exploitation is guaranteed
- **Support for well-known parallel APIs (OpenMP and Pthreads)**
  - No need for special tools to split the application code
  - Automatic thread allocation

ILP exploitation

- **Dynamic Instruction Merging (DIM) technique**
  - Instruction level parallelism is transparently exploited
  - The DAP processor adapts to the application ILP, so it can emulate the behavior of the dedicated accelerators





Advantages

- Platform update does not rely on source code modifications
- Easy software development process
- Adaptability

The DAP Processor

1. **Five-stage SparcV8 processor**
2. **Dynamic Instruction Merging Hardware**
   - Four-stage pipeline
   - Optimization over the binary code (Software Compatibility)

3 Reconfigurable Data Path

- Combinational Logic
- Tightly coupled
- On-the-fly Reconfiguration

4 Reconfiguration Memory (RM)

- Store the translated code generated by the DIM hardware

5 Address Cache

- 4-way Associative
- Index the translated code stored in the RM

Performance against Single Issue Processor

	MPSparcV8				CReAMS			
	4SparcV8	8SparcV8	16SparcV8	64SparcV8	4DAPs	8DAPs	16DAPs	64DAPs
	Speedup							
equake	1.57	1.74	1.86	1.93	2.11	2.34	2.48	2.58
apsi	1.59	1.77	1.87	1.92	2.02	2.25	2.37	2.43
ammp	1.42	1.51	1.58	2.02	2.69	2.95	3.15	4.38
susan_e	2.15	2.69	3.06	3.39	3.38	4.67	5.76	6.84
patricia	1.24	1.47	1.28	1.23	1.94	2.87	2.49	2.39
susan_c	2.98	4.60	6.29	8.77	4.59	7.77	11.90	19.88
susan_s	3.93	7.81	14.98	48.93	7.69	15.04	28.65	92.84
md	3.91	7.54	14.06	38.22	10.91	20.22	34.83	74.91
jacobi	3.92	7.78	15.24	50.97	5.57	11.00	21.41	69.74
lu	3.08	4.86	4.18	3.51	6.28	10.55	8.30	6.85
Average	***2.58***	***4.18***	***6.44***	***16.09***	***4.72***	***7.97***	***12.13***	***28.28***

Same Area Designs #1 *Same Area Designs #2*

EDP against Single Issue Processor

	MPSparcV8				CReAMS			
	4SparcV8	8SparcV8	16SparcV8	64SparcV8	4DAPs	8DAPs	16DAPs	64DAPs
	Energy-Delay Product (J*1e-3s)							
equake	293	305	287	343	169	175	162	149
apsi	10768	10386	10169	10282	6361	6143	6023	5355
ammp	19698	22155	20764	12814	5452	6282	5761	2984
susan_e	7.97	7.15	6.55	6.12	3.46	2.85	2.43	2.12
patricia	2.91	1.96	2.54	2.65	1.47	0.77	1.02	1.06
susan_c	1.0296	0.8134	0.6274	0.4624	0.5160	0.3761	0.2600	0.1600
susan_s	177.2	102.5	59.8	18.7	41.7	24.9	14.7	4.7
md	0.000282	0.000171	0.000098	0.000039	0.000066	0.000042	0.000026	0.000013
jacobi	35.09	20.67	11.33	3.61	17.37	10.27	5.67	1.85
lu	0.000124	0.000091	0.000127	0.000215	0.000041	0.000028	0.000043	0.000076

Same Area Designs #1 *Same Area Designs #2*

Conclusion

- The adaptability in exploiting ILP of CReAMS provides, on average, 34% of performance improvements and still reduces 2.2 times the energy consumption compared to a multiprocessor system composed of Single Issue SparcV8 processors when the same chip area is considered.
- CReAMS outperforms a multiprocessor system composed of 4-issue Out-of-Order processors in 18.25% when the same power budget is considered.

Execution Time against 4-issue OOO Superscalar

	4-issue OOO MPSparcV8		CReAMS	
	4SparcV8	8SparcV8	32DAPs	64DAPs
	Execution Time (ms)			
susan_c	16.448	11.221	12.838	10.344
swaptions	7.094	3.551	1.572	0.792
blackscholes	3.408	1.710	1.048	0.535
jacobi	123.841	62.245	33.665	19.233
lu	0.352	0.265	0.279	0.310

Same Power Budget #1 Same Power Budget #2

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