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PARALLEL PIPELINE SOLUTION FOR HARDWARE IMPLEMENTATION OF ARTIFICIAL NEURAL NETWORKS WITH IN CIRCUIT REAL TIME WEIGHT UPDATE

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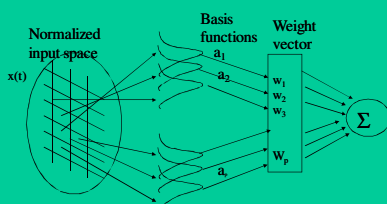
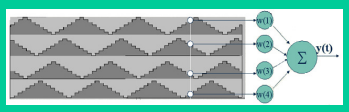
INTRODUCTION: The FPGA circuits meet more and more different types of applications for real-time operational implementation. From the point of view of hardware implementation of artificial neuronal networks, the FPGA circuits represent a suitable, non-negligible, efficient hardware support.
In this paper the parallel pipeline hardware model of different types of artificial neural networks are presented, with efficient utilization of FPGA circuit resources.
The presented parallel-pipeline models provide real-time calculation of the network output and the weight update.

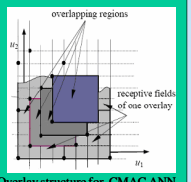
For RBF-ANN and for Kohonen SOM the weight adaptation is realised in parallel with the network output calculation.
The resulted architecture of CMAC, RBF and Kohonen SOM can be compared based on the architecture presented in the figures.
The use of combination of different types of design (Xilinx ISE Project Navigator, Embedded Development Kit, Xilinx System Generator) and testing (ChipScope Pro Analyzer) tools and methodologies allows rapid prototyping and start-up of hardware implementation of artificial neural networks.
The embedded processor cores are useful in handling the network parameters, weight initialization, weight storage, in the testing process of the hardware implemented ANN.
The ANNs were implemented in VHDL, the IP cores were generated with System Generator. The resulted IP cores with artificial neural networks were integrated on the bus (PLB, AXI) of the embedded processor cores.

CMAC-ANN Cerebelar Model Articulation Controller Artificial Neural Network

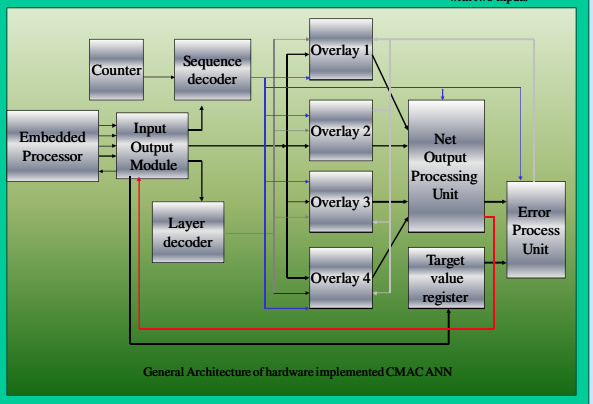


General Architecture of CMAC ANN

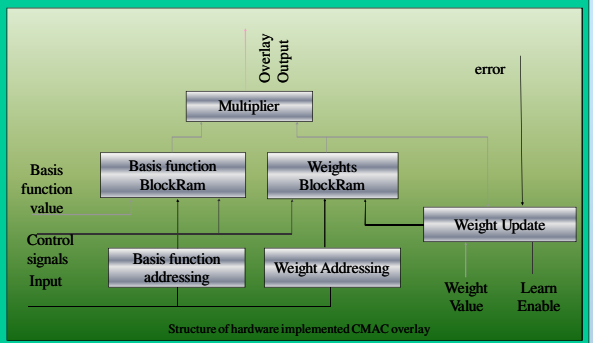

Overlay structure for single input CMAC



Overlay structure for CMAC ANN with two inputs

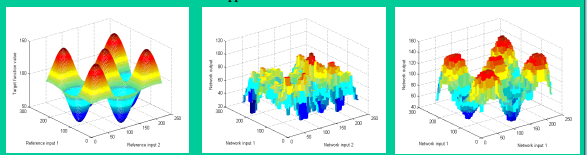


General Architecture of hardware implemented CMAC ANN



Structure of hardware implemented CMAC overlay

Surface approximation with CMAC ANN

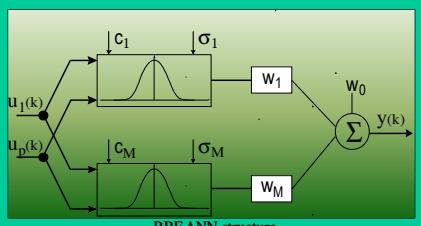

Target surface | Surface after first training cycle | Surface after training cycle 20

The developed network is very fast, in 8 clock cycles the network output and weight update is processed regardless of the number of network inputs.

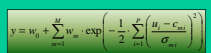
Hardware implemented ANN characteristics:
- Implementation of the artificial neural networks in VHDL
- Fixed point arithmetic for data representation
- Scalable architectures with GENERIC parameters
- Easy integration in real application with Simulink System Generator

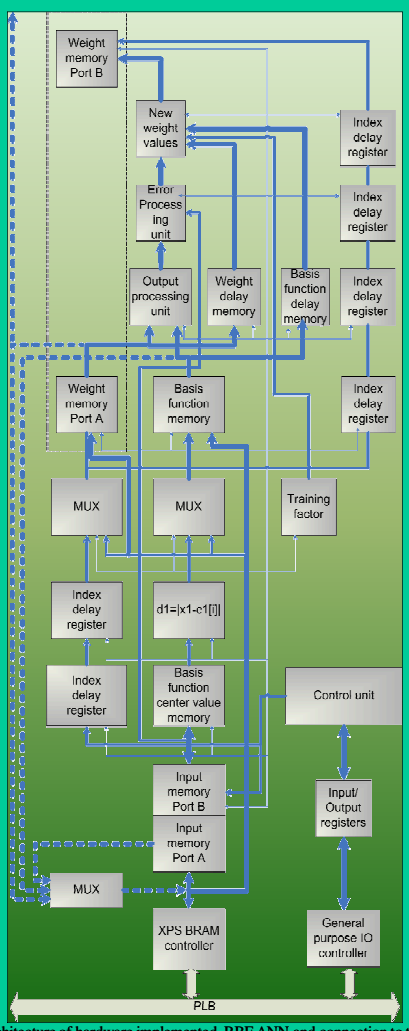
Used FPGA chips XILINX SPARTAN 3, XILINX SPARTAN 3E, XILINX SPARTAN 6, Virtex II Pro, Virtex V.

RBF-ANN Radial Basis Function Artificial Neural Network



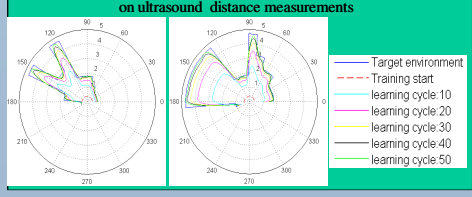
RBF ANN structure


RBF ANN output processing

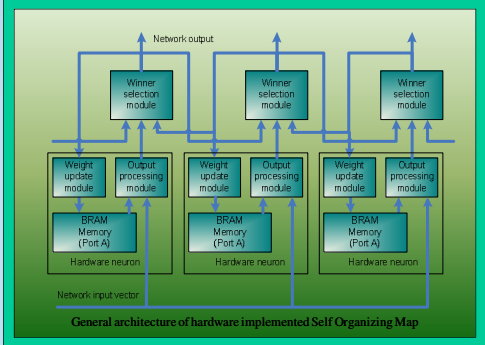


Architecture of hardware implemented RBF ANN and connection to the embedded processor PLB bus

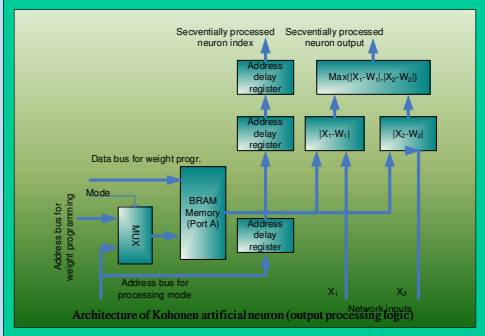
Example of application of RBF ANN for environment modeling based on ultrasound distance measurements



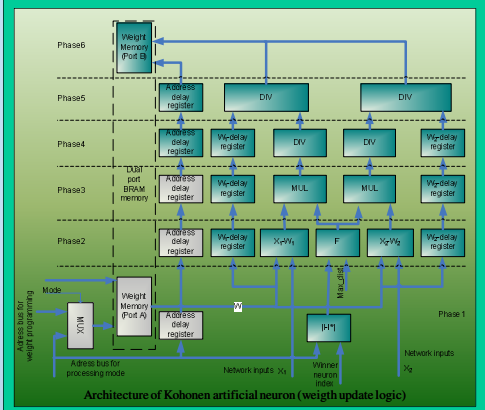
Kohonen SOM -Self Organizing Map



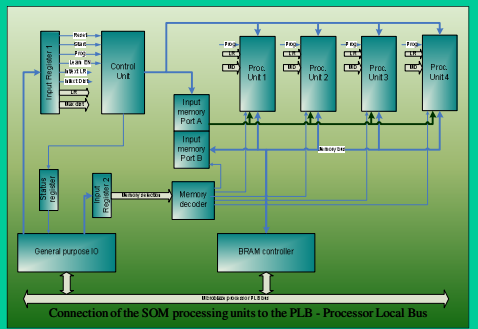
General architecture of hardware implemented Self Organizing Map



Architecture of Kohonen artificial neuron (output processing logic)



Architecture of Kohonen artificial neuron (weigth update logic)



Connection of the SOM processing units to the PLB - Processor Local Bus

Application of hardware implemented Kohonen network for path planning of an autonomous mobile robot

ACKNOWLEDGEMENT

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