HETEROGENEOUS CPU/FPGA COMPUTING SYSTEM FOR AVIONIC TEST APPLICATIONS

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Real-time computing systems are increasingly used in aerospace and avionic industries. In the face of power wall and real-time requirements, hardware designers are directed towards reconfigurable computing with the usage of heterogeneous CPU/FPGA systems. In such systems, multi-core CPU provides high computation rates while the reconfigurable logic offers high performance per watt and adaptability to the application constraints. Designers could exploit the existing partitioning in the application which leads to several feasible implementations with different performances. However, there is a lack of CAD tools able to deal with the development of applications on such heterogeneous systems dedicated to avionic Test and Simulation (T&S). This research investigates the problem of efficient mapping of real-time application on a CPU/FPGA architecture used to implement intimately coupled hardware and software avionic models. Our project includes the description of a heterogeneous CPU/FPGA environment and the corresponding design methodology. Experimental results underpin the relevance of the presented approach for testing avionic systems.