

DCIS'2001 Programme

Conference sessions

Wednesday, November 21

8:45 – 9:00 **Opening session**

9:00 – 10:00 **Plenary Session 1**

Wireless Systems-on-a-Chip Design
Prof. Robert Brodersen
Univ. California, Berkeley, USA

10:00 – 11:00 **Session 1a. Analogue Cells (I)**

Chairs: Carlos Leme, Chipidea (Portugal)
Diego Vazquez, Inst. de Microelectronica de Sevilla (Spain)

A Fully Differential CMOS Switched-Opamp for Low Voltage SC circuits

J. Arias¹, L. Enríquez¹, L. Quintanilla¹, J. Vicente¹, J. Barbolla¹, D. Vázquez² and A. Rueda²

¹E.T.S. de Ingenieros de Telecomunicación, Univ. de Valladolid, Spain

²Instituto de Microelectrónica de Sevilla, Centro Nacional de Microelectrónica, Univ Sevilla, Spain

A BiCMOS Fully Differential Integrator for Fast Pulse Discrimination

Sebastià Bota¹, Angel Diéguez¹ and David Gascón²

¹Dept. d'Electrònica, Univ. de Barcelona, Spain

²Dept. d'Estructura i Constituents de la Matèria, Univ. de Barcelona, Spain

Current Driver for Myocardial Impedance Measure

Alberto Yúfera and Adoración Rueda

Instituto de Microelectrónica de Sevilla, Centro Nacional de Microelectrónica, Univ Sevilla, Spain

10:00 – 11:00 **Session 1b. FPGA Tools**

Chairs: Horácio Neto, IST/INESC-ID (Portugal)
José Luis Martín, Univ. Pais Vasco (Spain)

Applying PADGP to the Problem of Placement and Routing on FPGAs

F. Fernández¹, J. M. Sánchez² and M. Tomassini³

¹Centro Universitario de Mérida, Univ. de Extremadura, Spain

²Escuela Politécnica, Univ. de Extremadura, Spain

³Institute d'Informatique, Univ. de Lausanne, Switzerland

Debugging and Tracing in JTAG-Compatible FPGA-Based Designs

M. García, A. de Castro, E. de la Torre, T. Riesgo and J. Uceda

Univ. Politécnica de Madrid, E.T.S.I. Industriales. División de Ingeniería Electrónica, Spain

HADES-1: A Rapid Prototyping Environment Based on Advanced FPGA's

M. A. Aguirre, J. N. Tombs, A. Torralba and L. G. Franquelo

Dept. de Ingeniería Electrónica, Escuela Superior de Ingenieros de Sevilla, Spain

10:00 – 11:00 Session 1c. System Level Modelling

Chairs: Manuel Bellido, Inst. de Microelectrónica de Sevilla (Spain)
José Augusto Lima, Univ. Minho, (Braga Portugal)

A System Specification Experiment with Esterel

Lluís Ribas, Joaquín Saiz and Jordi Carrabina
Dept. d'Informàtica, Escola Tècnica Superior d'Enginyeria, Univ. Autònoma de Barcelona, Spain

VHDL model of a 16/32-bit ALU based on asynchronous logic

José L. Martín, Jaime Jiménez and Gerardo Aranguren
Dept. de Electrónica y Telecomunicaciones, Univ. del País Vasco, Spain

An Energy Model and Estimator for a 32 Bit Microprocessor

G. Caldentey, J. Cid, J. Rius, S. Manich and R. Rodriguez
Dept. d'Enginyeria, Univ. Politècnica de Calanunya, Spain

11:00 – 11:30 Coffee break

11:30 – 12:30 Session 2a. Integrated Filters

Chairs: Manuel Medeiros Silva, IST/INESC-ID (Portugal)
Francisco Duque, Univ. Extremadura (Spain)

Programmable SC Biquad Using One Single Capacitor Bank

A. Torralba, A. P. Vegaleal and L. G. Franquelo
Dept. de Ingeniería Electrónica, Univ. Sevilla, Spain

A Switched-Capacitor Bandpass Filter with Quasi-Continuous Q-Factor Tunability

J. L. Ausín, J. F. Duque-Carrillo, R. Pérez-Aloe and J. V. Sánchez
Dept. Ingeniería Electrónica y Electrotécnica, Univ. de Extremadura, Spain

A 10.7MHz FGMOS Low Power Sixth Order Bandpass Filter

Esther O. Rodríguez-Villegas, Adoración Rueda and Alberto Yúfera
Instituto de Microelectrónica de Sevilla, Centro Nacional de Microelectrónica, Univ. Sevilla, Spain

11:30 – 12:30 Session 2b. Digital Numerical ICs

Chairs: Luis Entrena, Univ. Carlos III de Madrid (Spain)
João Canas Ferreira, Univ. Porto (Portugal)

A Methodology and Tool to Design Optimized Standard Cell Based M x N Signed Multipliers

H. Souffi-Kebbat, J. Ph. Blonde and F. Braun
Laboratoire d'Electronique et de Physique des Systèmes Instrumentaux, Strasbourg, France

A Comparison of Switching Noise Generation in CMOS Binary Parallel Adders

P. Parra, A. Acosta, C. Jiménez and M. Valencia
Instituto de Microelectrónica de Sevilla, Centro Nacional de Microelectrónica, Univ. Sevilla, Spain

Analysis of the Number of Multipliers in Radix-2 FFT Modules with Different Latency and Area Constraints.

J. A. López, J. M. Díez and C. Carreras
Dept. Ingeniería Electrónica, E.T.S.I. Telecomunicación, Univ. Politécnica de Madrid, Spain

11:30 – 12:30 Session 2c. HW/SW Codesign

Chairs: Juan Carlos López, Univ. Castilla-La Mancha (Spain)
Yago Torroja, Univ. Politecnica de Madrid (Spain)

A New Co-Design Methodology for Embedded Signal Processing Systems

Mário P. Véstias and Horácio Neto
INESC-ID / IST, Lisboa, Portugal

Hardware-Software Co-design of a Cryptographic Application

Diego Matilla¹, Marisa Lopez-Vallejo¹ and Ander Royo²

¹Dept. Ingeniería Electrónica, E.T.S.I. Telecomunicación, Univ. Politécnica de Madrid, Spain

²Agere Systems, Pol. Industrial Tres Cantos, Spain

DEMETER: A Novel Framework for Hardware and Software System Specification, Simulation and Verification in C++

Héctor Navarro, Juan. A. Montiel-Nelson, Javier Sosa and R. Sarmiento

Research Institute for Applied Microelectronics, Univ. de Las Palmas de Gran Canaria, Spain

12:30 – 14:30 Lunch

14:30 – 15:50 Session 3a. Access in Communication Systems

Chairs: Rafael Burriel, IBIT (Spain)
Juan A. Montiel Nelson, Univ. Las Palmas de Gran Canaria (Spain)

A Narrow Band Power Line Communications System in a Single Device

J. I. García-Nicolás, I. Urriza, A. Sanz, J. I. Artigas and A. Valdovinos
Dept. of Electronics and Communication Engineering, Univ. Zaragoza, Spain

Virtual Components Design for Wireless Communications Using PCMCIA Interfaces

Antoni Portero, Antonio Nuñez and Jordi Carrabina
Univ. Autònoma de Barcelona, Spain

Integration of Advance Encryption Standard in Smart Cards

Raul Sanchez-Reillo
Dept. Ingeniería Eléctrica, Electrónica y Automática, Univ. Carlos III de Madrid, Spain

OFDM Synchronization Scheme for Power Line Telecommunications (PLT)

V. Baena, J. Granado, M. A. Aguirre, A. Torralba and L. G. Franquelo
Dept. de Ingeniería Electrónica, Univ. Sevilla, Spain

14:30 – 15:50 Session 3b. Logic and High-Level Synthesis

Chairs: Jose Manuel Mendias, Univ. Complutense de Madrid (Spain)
Lluís Ribas, Univ. Autònoma de Barcelona (Spain)

Experiments in Rapid Prototyping of Reactive Systems with POLIS

Moisés Serra¹, Jordi Tirado², Joaquín Saiz³, Lluís Ribas³ and Jordi Carrabina³

¹Dept. d'Electrònica i Telecomunicacions, Univ. de Vic, Spain

²Calmell, S. A., Spain

³Dept. Informàtica, ETSE, Univ. Autònoma de Barcelona, Spain

Multiple-Precision Circuits Allocation Independent of Data-Objects Length

M. C. Molina, J. M. Mendías and R. Hermida

Dept. Arquitectura de Computadores y Automática, Univ. Complutense de Madrid, Spain

Some of the Capabilities of Redundancy Addition and Removal Applied to Sequential Logic Circuits

Enrique San Millán, Luis Entrena and José Alberto Espejo
Dept. Ingeniería Eléctrica, Electrónica y Automática, Univ. Carlos III de Madrid, Spain

A Flexible State Assignment Algorithm for Low Power Implementations

Manuel Martínez¹, María J. Avedillo^{1,2}, José M. Quintana^{1,2} and José L. Huertas^{1,2}
Instituto de Microelectrónica de Sevilla, Centro Nacional de Microelectrónica, Spain
Dept. de Electrónica y Electromagnetismo, Univ. Sevilla, Spain

14:30 – 15:50 Session 3c. Analogue Circuit Testing

Chairs: Carlos Beltran Almeida, INESC-ID (Portugal)
José Luis Huertas, Inst. de Microelectrónica de Sevilla (Spain)

Filter Based-BIST for SINAD Measurement of A/D Converter

Ch. Rebai, D. Dallet and Ph. Marchegay
IXL Laboratory – ENSEIRB, Univ. of Bordeaux I, France

Oscillation-Test Technique for CMOS OpAmps by Monitoring Supply Current

J. Font, J. Ginard, E. Isern, M. Roca and E. García
Dept. de Física, Univ. Illes Balears, Palma de Mallorca, Spain

A New BIST Scheme for Sigma-Delta Modulators

J. Machado da Silva, J. S. Duarte and J. S. Matos
INESC Porto, Univ. do Porto, Portugal

On-Chip Evaluation of Oscillation Based Test Output Signals for Switched-Capacitor Circuits

Diego Vázquez, Gloria Huertas, Gildas Leger, Eduardo Peralías, Adoración Rueda, José Luis Huertas
Instituto de Microelectrónica de Sevilla, Centro Nacional de Microelectrónica, Univ. Sevilla, Spain

15:50 – 16:10 Coffee break

16:10 – 17:30 Session 4a. Modelling and CAD (I)

Chairs: Nadine Azemard, LIRMM (France)
Eugeni Isern, Univ. Islas Baleares (Spain)

Large-Signal Nonlinear Model for MESFET Triode and Saturation Zones

Nuno Borges de Carvalho and José Carlos Pedro
Inst. de Telecomunicações, Univ. de Aveiro, Portugal

SiDSen: A Program to Simulate Delays Based on Sensitivity Analysis Model

J. García, J. Pulido, A. Hernández, J. del Pino, B. González, J. R. Sendra and A. Nunez
Dept. de Ingeniería Electrónica y Automática, Instituto Univ. de Microelectrónica Aplicada, Univ. de Las Palmas de Gran Canaria, Spain

Method of Frequency Adjusting for Transient Noise Analysis of Nonlinear Circuits

M. M. Gourary¹, S. G. Rusakov¹, S. L. Ulyanov¹, M. M. Zharov¹ and B. J. Mulvaney²
¹IPPM, Russian Academy of Science, Moscow, Russia
²Motorola Inc., Austin, Texas, USA

Layout-Constrained Retargeting of Analog Blocks

R. Castro-López, F. V. Fernández, M. Delgado-Restituto, F. Medeiro and A. Rodríguez-Vázquez
Instituto de Microelectrónica de Sevilla, Centro Nacional de Microelectrónica, Spain

16:10 – 17:30 Session 4b. Integrated Sensors

Chairs: Jaume Segura, Univ. Islas Baleares (Spain)
 António Cruz Serra, IST, Lisboa (Portugal)

CMOS Only Magnetic Sensor with an Enhanced Sensitivity Interface Circuit

E. Montané, D. Celma, G. Hornero, S. A. Bota and J. Samitier
Instrumentation and Communication Systems, Univ. de Barcelona, Spain

ACE16K: a Programmable Analog Array for Focal-Plane Vision Applications

G. Liñán, R. Domínguez-Castro, S. Espejo and A. Rodríguez-Vázquez
Instituto de Microelectrónica de Sevilla, Centro Nacional de Microelectrónica, Spain

CMOS Optical Receivers for Fiber Communications

G. Chapinal, G. Hornero, E. Montane, M. Moreno, A. Herms and J. Samitier
Laboratori de Sistemes d'Instrumentació i Comunicacions, Dept. d'Electrònica, Univ de Barcelona, Spain

A CMOS Linear Photosensor Array for Telemetric Applications

G. Hornero, E. Montane, G. Chapinal, R. Meri, M. Moreno and A. Herms
Instrumentation and Communication Systems, Univ. de Barcelona , Spain

16:10 – 17:30 Session 4c. FPGA Applications (I)

Chairs: Juan J. Rodriguez Andina, Univ. Vigo (Spain)
 António Ferrari, Univ. Aveiro (Portugal)

Minimum Latency NURBS to Bézier Converter

P. N. Mallón, M. Bóo and J. D. Bruguera
Dept. of Electronic and Computer Engineering, Univ. of Santiago de Compostela, Spain

RNS Based PID Controllers with Adaptive Support over FPL Devices

Luis Parrilla¹, Javier Ramírez¹, Antonio García¹, Pedro G. Fernández² and Antonio Lloris¹

¹Dept. Electrónica y Tecnología de Computadores, Univ. de Granada, Spain

²Dept. Ingeniería Eléctrica, Univ. de Jaén, Spain

FPGA Implementation of a MIPS Processor

Betariz Ruiz and Pablo Sanchez
Microelectronics Engineering Group, Univ. of Cantabria

Could FPGAs Be Used to Classify Cork Stoppers? An Experimental Study

Miguel A. Vega-Rodríguez, Juan M. Sánchez-Pérez and Juan A. Gómez-Pulido
Dept. de Informática, Escuela Politécnica, Univ. de Extremadura, Cáceres, Spain

16:10 – 17:30 Session 4d. High-Level Testing

Chairs: Emilio Olías, Univ. Carlos III de Madrid (Spain)
 José Vieira dos Santos, ISEP, Porto (Portugal)

Automatic Insertion of Fault-Tolerant Structures at the Register Transfer Level

Celia López, Luis Entrena and Emilio Olías
Electronic Technology Area, Univ. Carlos III de Madrid, Spain

Exploring Test Solutions by Means of System-Level Design Tools

M. Lajolo¹, M. Sonza Reorda² and M. Violante²

¹NEC C&C Research Labs, Princeton, NJ, USA

²Dipt. di Automatica e Informatica, Politecnico di Torino, Italy

Synthesizable VHDL Model of a Boundary-Scan Tester

Ángel Quirós Olozábal, Diego Gómez Vela, Francisco Lucas Fernández and Carmen García López
Grupo de Diseño de Circuitos Microelectrónicos, Univ. de Cádiz, Spain

An Interpretation Framework for Evaluating High-Level Fault Models and ATPG Capabilities

Fulvio Corno, Matteo Sonza Reorda and Giovanni Squillero

Dipt. di Automatica e Informatica, Politecnico di Torino, Italy

17:45 – 19:00 **Panel session 1**

European Research: Present and Future Strategies

Moderator: Javier Uceda, Univ. Politécnica de Madrid, Spain

Thursday, November 22

9:00 – 10:00 **Plenary Session 2**

Mixed-Signal Testing and Design-For-Test in the Deep Submicron Age

Prof. Linda Milor

Georgia Tech, USA

10:00 – 11:00 **Session 5a. Analogue Cells (II)**

Chairs: Francisco Fernandez, Inst. de Microelectronica de Sevilla (Spain)

Santiago Celma, Univ. Zaragoza (Spain)

An Independent Inversion Transistor Level Constant- g_m Technique for Low-Voltage Rail-to-Rail Amplifiers

Juan M. Carrillo, José L. Ausín, and J. F. Duque-Carrillo

Dept. of Electronics and Electrical Engineering, Univ. of Extremadura, Badajoz, Spain

Low-Voltage Differentiator for VHF Filtering

C. Aldea, S. Celma and A. Otín

Grupo de Diseño Electrónico, Facultad de Ciencias, Univ. de Zaragoza, Spain

Dynamic Performance of Parallel -Type ADCs with Different Encoders

Paula Pereira^{1,3} and Jorge R. Fernandes^{2,3}

¹Dept. Eng. Electr., Escola Superior de Tecnologia, IPCB, Castelo Branco, Portugal

²Instituto Superior Técnico, Lisboa, Portugal

³INESC-ID, Lisboa, Portugal

10:00 – 11:00 Session 5b. Digital Design

Chairs: Eugenio Villar, Univ. Cantabria (Spain)
Celia López, Univ. Carlos III de Madrid (Spain)

Design of a Trigonometric Coprocessor with VHDL Based on Delay-Insensitive Logic

José L. Martín, Gerardo Aranguren and Jaime Jiménez
Dept. de Electrónica y Telecomunicaciones, Univ. del País Vasco, Bilbao, Spain

Verification of a Digital Video Broadcasting Satellite System

Victor Fernández¹, Luis Berrojo², Josep Prat² and Yves Leroy²
¹Dept. of Electronics Technology, System and Automation Engineering, Univ. of Cantabria, Santander, Spain
²Alcatel Espacio, Madrid, Spain

A Comparative Evaluation of an Asynchronous Implementation on FPGAs

Rubén Alarcón and Jordi Carrabina
Univ. Autònoma de Barcelona, ETSE, Spain

10:00 – 11:00 Session 5c. FPGA Applications (II)

Chairs: Valeri Skliarov, Univ. Aveiro (Portugal)
Eduardo de la Torre, Univ. Politecnica de Madrid (Spain)

Taking Advantage of FPGAs to Implement Fieldbus Interfaces

M. D. Valdés, M. A. Domínguez, M. J. Moure and G. Lías
Institute of Applied Electronics, Dept. of Electronic Technology, Univ. of Vigo, Spain

FPGA Based Development Vision System

Pedro Cobos Arribas¹ and F. Monasterio-Huelin Maciá²
¹Dept. de Sistemas Electrónicos y de Control, EUIT Telecomunicación, Univ. Politécnica de Madrid, Spain
²Dept. de Tecnologías Aplicadas a la Telecomunicación, ETSI Telecomunicació, Univ. Politécnica de Madrid, Spain

Scalable RSA Processor in Reconfigurable Hardware - a SoC Building Block

Viktor Fischer¹ and Milos Drutarovský²
¹Laboratoire Traitement du Signal et Instrumentation, Univ. Jean Monnet, Saint-Etienne, France
²Dept. of Electronics and Multimedia Communications, Tech. Univ. of Kosice, Slovak Republic

11:00 – 11:30 Coffee break

11:30 – 12:30 Session 6a. Circuit Analysis Techniques

Chairs: Adoracion Rueda, Inst. de Microelectronica de Sevilla (Spain)
Fernand Michel Roche, LIRMM, Univ. Montpellier II (France)

A Tool for Teaching/Learning the Behavior of Analog Integrated Circuits

José Fariña, JuanJ. Rodríguez-Andina and Luis G. Samartín
Dept. of Electronic Technology, Univ. of Vigo

A New High Voltage Operational Amplifier Designed to Drive Piezoelectric Actuators for Microrobotic Applications

E. Montané, P. Miribel, S. A. Bota, M. Puig-Vidal and J. Samitier
Instrumentation and Communication Systems, Univ. de Barcelona, Spain

Analysis of High-Performance Flip-Flops for Mixed-Signal Applications

R. Jiménez¹, P. Parra², P. Sanmartín², and A. J. Acosta²

¹Dept. IESIA, Univ. de Huelva, Spain

²Instituto de Microelectrónica de Sevilla, Centro Nacional de Microelectrónica, Univ. Sevilla, Spain

11:30 – 12:30 Session 6b. Neural and Fuzzy Systems

Chairs: Antonio Torralba, Univ. Sevilla (Spain)
Armando Roy, Univ. Zaragoza (Spain)

Design and Implementation of a Membership Function Circuit in CMOS Technology

Leonardo Mesquita¹, Galdenoro Botura Jr.¹ and Osamu Saotome²

¹Dept. Engenharia Elétrica, Univ. Estadual Paulista, SP, Brasil

²Instituto Tecnológico de Aeronáutica, São José dos Campos, Brasil

VLSI Design of Universal Approximator Neuro-Fuzzy Systems

I. Baturone, S. Sánchez Solano, A. Barriga, C. J. Jiménez, R. Senhadji-Navarro and D. R. López
Instituto de Microelectrónica de Sevilla, Centro Nacional de Microelectrónica, Spain

A Fast, Configurable Digital Neural Network ASIC for High-Speed Applications

José Luis Ayala, Antonio G. Lomeña, Marisa López-Vallejo and Ángel Fernández
Dept. de Ingeniería Electrónica, Univ. Politécnica de Madrid, Spain

11:30 – 12:30 Session 6c. Analogue Circuit Modelling

Chairs: Christian Duzafa, LIRMM (France)
Raul Navas, Siemens (Germany)

E_G and X_{TI} Parameters Extraction Method Using Direct Measurement of Process Temperature

W. Rahajandraibe¹, C. Dufaza¹, D. Auvergne¹, B. Cialdella², B. Majoux² and V. Chowdhury²

¹LIRMM, Univ. de Montpellier II, France

²ST-Microelectronics, Grenoble, France

Modelling and Automatic Generation Tool for Integrated Inductors in CMOS Technology

J. del Pino¹, J. R. Sendra¹, A. Hernández¹, S. L. Khemchandani², J. Aguilera, B. González¹, J. García¹
and A. Nunez¹

¹Dept. de Ingeniería Electrónica y Automática, Univ. de Las Palmas de Gran Canaria, Spain

²INCIDE Canary S.A., Las Palmas, Spain

Study of Non-Linear S/H Operation in Switched-Current Circuits using Volterra Series - Application to Bandpass Sigma-Delta Modulators

J. M. de la Rosa, B. Pérez-Verdú, F. Medeiro, R. del Río and A. Rodríguez-Vázquez
Instituto de Microelectrónica de Sevilla, Centro Nacional de Microelectrónica, Spain

12:30 – 14:30 Lunch

14:30 – 15:50 Session 7a. Modelling and CAD (II)

Chairs: Christian Jay, Infineon (France)
Fulvio Corno, Politecnico de Torino (Italy)

Applying Data Mining Techniques to Tune System Scheduling

Antonio G. Lomeña, Marisa López Vallejo and Antonio García Quintas
Dept. de Ingeniería Electrónica, Univ. Politécnica de Madrid, Spain

Study of Different Kind of Tools to Analyse the Quality of HDL Designs. Comparison of Their Coverage of the RMM Guideline.

Fernando Casado¹, Felipe Machado¹, Natividad Martínez², Yago Torroja¹, Peter Neumann³ and Ralf Seepold²

¹ETSI Industriales, Univ. Politécnica de Madrid, Spain

²Forschungszentrum Informatik, Univ. Karlsruhe, Germany

³SCI-WORX, Hanover, Germany

A Datapath Generator for Bit Slice Architectures

J. Sosa, Juan A. Montiel-Nelson, Hector Navarro-Botello, V. de Armas and R. Sarmiento
Research Institute for Applied Microelectronics, Univ. de Las Palmas de Gran Canaria, Spain

ISS: Interactive Simulation System

P. Ruiz-de-Clavijo, M. J. Bellido Diaz, J. Juan-Chico and C. Baena Oliva

Instituto de Microelectrónica de Sevilla, Centro Nacional de Microelectrónica, Univ. of Sevilla, Spain

14:30 – 15:50 **Session 7b. Industrial DSP Implementations**

Chairs: Antonio Núñez, Univ. Las Palmas de Gran Canaria (Spain)
J. Ignacio Martínez Torre, Univ. Rey Juan Carlos (Spain)

M3Recorder: A MP3 Encoding Based Recorder

J. M. Flores, M. Montón, A. Núñez and A. J. Velasco
Dept. Informàtica, Univ. Autònoma de Barcelona, Spain

The DSP Implementation of the AES Encryption Algorithm

Slobodan Bojanic and O. Nieto-Taladriz Garcia
Dept. de Ingeniería Electrónica, ETSI Telecomunicación, Univ. Politécnica de Madrid, Spain

Rapid Prototyping of MC-CDMA Transmission Technique on HW/SW Architecture

Sébastien Le Nours, Fabienne Nouvel and Jean-François Hèlard
Lab. For Components and Systems of Telecommunications, INSA, Rennes, France

Image Acquisition and Digitalizing System for an Electronic Voting System

J. L. Martín, J. Lázaro, U. Bidarte, A. Zuloaga, K. Espinosa and I. Goirizelaia
Dept. de Electrónica y Telecomunicaciones, Univ. del País Vasco, Bilbao, Spain

14:30 – 15:50 **Session 7c. BIST and Boundary Scan**

Chairs: Salvador Bracho, Univ. Cantabria (Spain)
João Paulo Teixeira, IST/INESC-ID (Portugal)

Experimenting the 1149.1 and 1149.4 Test Infrastructures in a Web-Accessible Remote Lab (Without Plug-ins!)

André Vaz Fidalgo^{1,2}, Ricardo J. Costa², Gustavo R. Alves^{1,2} and José M. Ferreira²

¹Instituto Superior de Engenharia do Porto, Portugal

²Faculdade de Engenharia da Universidade do Porto, Portugal

Using Tabu Method for Optimizing the Cost of Hybrid BIST

Raimund Ubar¹, Helena Kruus¹, Zebo Peng² and Gert Jervan²

¹Technical Univ. of Tallinn, Estonia

²Univ. of Linköping, Sweden

Low Energy Built-In Self-Test Preparation at RT-Level

M. B. Santos¹, J. Braga¹, P. Coimbra¹, J. P. Teixeira¹, S. Manich², L. Balado² and J. Figueras²

¹IST / INESC-ID, Lisboa, Portugal

²Univ. Politecnica de Catalunya, Barcelona, Spain

15:50 – 16:10 Coffee break

16:10 – 17:30 Session 8a. RF Circuits

Chairs: Dinis Santos, Univ. Aveiro (Portugal)
Joan Ramon Morante, Univ. de Barcelona (Spain)

Isolation Improvement of Silicon Double Balanced RF Mixer using Micromachining Techniques

J. Cabanillas, J. M. Lopez-Villegas, J. Sieiro, J. A. Osorio and J. Samitier
Laboratori de Sistemes d'Instrumentació i Comunicació, Dept. d'Electrònica, Univ de Barcelona, Spain

A 2.5V, 10 GHz Fully Integrated LC-VCO with 30% Tuning Range

Wouter De Cock and Michiel Steyaert
Dept. ESAT-MICAS, Katolieke Univ. Leuven, Belgium

A 2 GHz Low Power CMOS Active Load Body Effect Mixer

Tierry Taris, Yann Deval, Jean-Baptiste Bégueret and Pascal Fouillat
IXL Laboratory – ENSEIRB, Univ. of Bordeaux I, France

A 1.575 GHz SiGe Low Noise Amplifiers for GPS Applications

J. del Pino¹, S. L. Khemchandani², A. Hernández¹, J. R. Sendra¹, J. García¹, B. González¹ and A. Núñez¹

¹Dept. de Ingeniería Electrónica y Automática, Univ. de Las Palmas de Gran Canaria, Spain

²INCIDE Canary S.A., Las Palmas, Spain

16:10 – 17:30 Session 8b. Reconfigurable Systems

Chairs: Henrique Santos, Univ. Do Minho (Portugal)
Viktor Fischer, Univ. Saint-Etienne (France)

Hierarchical Specification and Implementation of Combinatorial Algorithms Based on RHS Model

Valery Sklyarov, Ioulia Skliarova and António B. Ferrari
Dept. of Electronics and Telecommunications, Univ. of Aveiro, Portugal

RED: A Reconfigurable Datapath

Fernando Rincón, José M. Moya and Juan Carlos López
Dept. de Informática, Univ. de Castilla-La Mancha, Spain

A Simulation Tool for a Pipelined SAT Solver

R. C. Ripado and J. T. de Sousa
INESC-Lisboa / IST, Lisboa, Portugal

A HW/SW Co-design Case Study: Implementing a Cryptographic Algorithm in a Reconfigurable Platform

Ivan González, Francisco J. Gómez and Javier Martínez
Lab. de Microelectrónica, ETSI, Univ. Autónoma de Madrid, Spain

16:10 – 17:30 Session 8c. DSP Methodologies

Chairs: Jordi Carrabina, Univ. Autónoma de Barcelona (Spain)
Francisco Restivo, Univ. Porto (Portugal)

Web-Based Configurable DSP Cores Delivery System Accelerated with Formal Verification

Alexa Vignollet and Pierre Bricaud
Mentor Graphics, France

Hardware Implementation of the Discrete Forward Wavelet Transform with Handel-C

José I. Martínez Torre and Jean-Pierre Deschamps
ESCET, Univ. Rey Juan Carlos, Móstoles, Spain

A New Methodology to Determine Minimum Arithmetical Formats (MAF's) for Fixed Point DSP Algorithms Computation

Mrcedes Pérez-Castellanos and Consuelo Gonzalo-Martín
DATSI, Fac. de Informática, Univ. Politécnica de Madrid, Spain

Morphological Processor for Real Time Image Processing

F. González, O. Tubío, F. Tobajas, V. De Armas, R. Esper-Chaín and R. Sarmiento
Instituto Universitario de Microelectrónica Aplicada, Univ. de Las Palmas de Gran Canaria, Spain

16:10 – 17:30 Session 8d. Regular Structures Test

Chairs: Joan Figueras, Univ. Politécnica de Catalunya (Spain)
Ana Leão, Infineon (Portugal)

Detecting Delay Coupling Faults within Memories

Mohamed Azimane¹, and Antonio Lloris Ruiz²
¹Philips Research Laboratories, Eindhoven, The Netherlands
²Dept. of Electronics and Computer Technology, Univ. of Granada, Spain

Monitoring and Analysis of Electrical Failures in Memory components Caused During Packaging

Ana Leão, Rui Pedro Silva and João Morais
Infineon Technologies F.S., Vila do Conde, Portugal

VHDL Fault Injection of SEUs in FPGA Based Fuzzy Logic Controller

O. Calvo¹ and R. Velazco²
¹LEICI - UNLP, Univ. de las Islas Baleares, Palma de Mallorca, Spain
²TIMA Laboratory, Grenoble, France

DRAFT: An On-line Concurrent Test for Partial and Dynamically Reconfigurable FPGAs

Manuel G. Gericota¹, Gustavo R. Alves¹, Miguel L. Silva² and José M. Ferreira²
¹Instituto Superior de Engenharia do Porto, Portugal
²Faculdade de Engenharia da Universidade do Porto, Portugal

17:45 – 19:00 Panel session 2

University and Industry Cooperation: Education and Research
Moderator: Pedro Guedes de Oliveira, INESC Porto, Portugal

Friday, November 23

9:00 – 10:00 Plenary Session 3

CMOS Multi-Standard Transceivers for Wireless Communications
Prof. Mohammed Ismail
Ohio-State University, USA

10:00 – 11:20 Session 9a. Analogue Techniques

Chairs: Chairs: Angel Rodriguez-Vázquez, Inst. de Microelectrónica de Sevilla (Spain)
João Vital. Chipidea (Portugal)

Stability of Feedback Laser Driver with the Average Power Control
P. Zivojinovic, M. Lescure and H. Tap-Béteille
ENSEEIH, Toulouse, France

Bandwidth Aspects in Second Generation Current Conveyors
Luís Nero Alves^{1,2}, Rui L. Aguiar¹ and Dinis M. Santos¹
¹Inst. de Telecomunicações, Univ. de Aveiro, Portugal
²ESTG, Instituto Politécnico de Leiria, Portugal

A Current Reference Circuit for Smart Power Technologies
E. Montané, S. A. Bota, P. Miribel-Català, M. Puig-Vidal and J. Samitier
Instrumentation and Communication Systems, Univ. de Barcelona, Spain

Fast Transient Statistical Evaluation of Analog Circuits
Rafael López-Ahumada and Rafael Rodríguez-Macías
Dept. IESIA, Univ. de Huelva, Spain

10:00 – 11:20 Session 9b. ICs for Control in Power Electronics

Chairs: Josep Samitier, Univ. de Barcelona (Spain)
José Manuel Quero, Univ. Sevilla (Spain)

FPGA-Based Control of a Flyback Converter with Power Factor Correction
A. de Castro, P. Zumel, O. García, T. Riesgo and J. Uceda
Univ. Politécnica de Madrid, E.T.S.I. Industriales. División de Ingeniería Electrónica, Spain

Conception of a Microrobot Unit Driven by Smart Power Integrated Circuits
E. Montané¹, P. Miribel-Català¹, S. A. Bota¹, J. López-Sánchez¹, M. Puig-Vidal¹, J. Samitier¹, U. Simu²
and S. Johnsson²
¹Instrumentation and Communication Systems, Univ. de Barcelona, Spain
²Dept. of Material Science, Univ. of Uppsala, Sweden

Design of a Processor Dedicated to AC Motor Control in a Multiprocessor Structure
H. de la Vallée Poussin, J.-D. Legat, D. Grenier and F. Labrique
Dept. of Electrical Engineering, Univ. Catholique de Louvain, Belgium

Evaluation of an Electronic Ballast Circuit for HID Lamps with Passive Power Factor Correction
Christian Brañas, Francisco J. Azcondo and Salvador Bracho
Dept. of Electronics Technology, System and Automation Engineering, Univ. of Cantabria, Santander, Spain

10:00 – 11:20 Session 9c. Power Modelling

Chairs: Pablo Sanchez, Univ. Cantabria (Spain)
Daniel Auvergne, LIRMM (France)

Simulation-Driven Switching Activity Evaluation of CMOS Digital Circuits

C. Baena, J. Juan-Chico, M. J. Bellido, P. Ruiz-de-Clavijo, C. J. Jiménez and M. Valencia
Instituto de Microelectrónica de Sevilla, Centro Nacional de Microelectrónica, Univ. of Sevilla, Spain

Modeling the Input-Output Coupling Capacitor Effects on the CMOS Buffer Power Consumption

J. L. Rossello and Jaume Segura
Dept. of Physics, Univ. of Balearic Islands Palma de Mallorca, Spain

Switching Current Modelling in CMOS Inverter for Speed and Power Estimation

P. Maurine, R. Poirier, N. Azémard and D. Auvergne
LIRMM, Univ. de Montpellier II, France

Characterization and Optimised Use of Digital CMOS Library Cells for Low Switching Noise Generation

A. Acosta, P. Parra and M. Valencia
Instituto de Microelectrónica de Sevilla, Centro Nacional de Microelectrónica, Univ. of Sevilla, Spain

10:00 – 11:20 Session 9d. Current Testing

Chairs: Eugenio Garcia Moreno, Univ. Islas Baleares (Spain)
Antonio Rubio, Univ. Politècnica de Catalunya (Spain)

Built-In Sensor Based on the Time-Variation of the Transient Current Supply in Analogue Circuits

R. Mozuelos, M. Martínez and S. Bracho
Dept. of Electronics Technology, System and Automation Engineering, Univ. of Cantabria, Santander, Spain

Testing SOI CMOS ICs with Parametric Methods: a Fundamental Analysis

Benjamín Iñíguez¹, Jean-Pierre Raskin³, Pascal Simon³, Denis Flandre² and Jaume Segura⁴
¹DEEEA, ETSE, Univ. Rovira i Virgili, Tarragona, Spain
²Microelectronics and ³Microwave Labs, Univ. Catholique de Louvain, Belgium
⁴Dept. of Physics, Univ. of Balearic Islands Palma de Mallorca, Spain

An Off-Chip Sensor Architecture for Transient Current Testing

B. Alorda and J. Segura
Dept. of Physics, Univ. of Balearic Islands Palma de Mallorca, Spain

On the Design of Checkers for Single-Word Code Spaces

Juan J. Rodríguez-Andina¹ and Santiago Fernández-Gómez²
¹Dept. of Electronic Technology, Univ. of Vigo, Spain
²ATI Research Silicon Valley, Santa Clara, CA, USA

11:20 – 11:50 Coffee break

11:50 – 13:10 Session 10a. Special Architectures

Chairs: Mar Martinez, Univ. Cantabria (Spain)
Javier Uceda, Univ. Politecnica de Madrid (Spain)

Hardware Implementation of Node Linking Segmentation Algorithm

F. J. Coslado, P. Camacho, M. González and F. Sandoval
Dept. Tecnología Electrónica, ETSI de Telecomunicación, Univ. de Málaga, Spain

Flexicamera: Intelligent and Flexible Camera

O. Ferraz, J. M. Flores, R. Juvanteny, M. Monton, A. Nuñez, J. Tirado, D. Castells, A. Portero, L. Ribas, A. Romero, J. Saiz, J. Velasco and J. Carrabina
U. Microelectrónica, Dept. Informàtica, ETSE, Univ. Autònoma de Barcelona, Spain

High-Speed Double-Precision Computation of Reciprocation and Division

J. A. Piñeiro and J. D. Bruguera
Dept. de Electrónica y Computación, Univ. Santiago de Compostela, Spain

Robustness of CMOS Circuits Designed for Space and Terrestrial Environment

J. M. Dutertre and F. M. Roche
LIRMM, Univ. Montpellier II, France

11:50 – 13:10 Session 10b. ATM Applications

Chairs: Roberto Sarmiento, Univ. Las Palmas de Gran Canaria (Spain)
José Ruela, Univ. Porto (Portugal)

A Parallel Architecture Implementation of an ATM Traffic Classifier

Susana Holgado¹, Sergio López-Buedo¹ and Alan J. Pearmain²
¹ETSI, Univ. Autónoma de Madrid, Spain
²Dept. of Electronic Engineering, Univ. of London, UK

An FPGA Solution for ATM Switching Architecture

Alexandru Stoica¹, Alain Greiner¹ and Jean Pierre Gauthier²
¹Lab. d'Informatique, Univ. Paris 6, France
²CS Telecom, Fontenay aux Roses, France

Implementation of an ATM Transceiver over SDH with Add/Drop Function at 2.5 Gbps

O. Tubío, R. Esper-Chaín, F. González, F. Tobajas, V. de Armas, J. A. Montiel and R. Sarmiento
Instituto Universitario de Microelectrónica Aplicada, Univ. de Las Palmas de Gran Canaria, Spain

System-Level Specification in SystemC of a Residential Gateway

Victor Fernández, Eugenio Villar and Fernando Herrera
¹Dept. of Electronics Technology, System and Automation Engineering, Univ. of Cantabria, Santander, Spain

11:50 – 13:10 Session 10c. Interconnect Modelling

Chairs: Miquel Roca, Univ. Islas Baleares (Spain)
João Teixeira de Sousa, IST, Lisboa (Portugal)

Power Supply Lines Design Considering Self-Heating Phenomena

M. Casu and M. Graziano
VLSI Lab, Dept. of Electronics, Politecnico di Torino, Italy

Signal Reflections in Coupled On-Chip Interconnections

Miquel Roca¹, Francesc Moll² and Eugeni Isern¹
¹Dept. of Physics, Univ. of Balearic Islands Palma de Mallorca, Spain
²Dept of Electronic Engineering, Univ. Politecnica de Catalunya, Barcelona, Spain

Parametric Impacts on Simultaneous Switching Noise in ASICs

Alaa F. Alani
LSI Logic Europe, Berks, UK

High-Speed Logic Families Impact on Power Supply Noise Generation

M. Graziano, G. Masera, G. Piccinini and M. Zamboni
VLSI Lab, Dept. of Electronics, Politecnico di Torino, Italy

Chairs: Francisco Azcondo, Univ. Cantabria (Spain)
Leopoldo Garcia Franquelo, Univ. Sevilla (Spain)

12-Lead ECG Modulator and Demodulator Equipment for Telephony Transmission

S. L. Toral, B. Lara Aznar, J. M. Quero and L. G. Franquelo
Dept. de Ingeniería Electrónica, Univ. Sevilla, Spain

A System to Detect Electrode Breakages in Arc Furnaces

José Fariña¹, Juan J. Rodríguez-Andina¹, Javier Bullón² and Ángel Lorenzo²
¹Institute of Applied Electronics, Dept. of Electronic Technology, Univ. of Vigo, Spain
²Ferroatlántica I+D, A Coruña, Spain

Microsystem for Automotive Door Module

J. L. Merino¹, S. A. Bota¹, J. Samitier¹, B. Niessen², E. Cabruja³, X. Jordà³, J. Bausells³, A. Ferré⁴ and J. Bigorra⁴
¹Instrumentation and Communication Systems, Univ. de Barcelona, Spain
²Austria Mikro Systeme International, Milano, Italy
³Centro Nacional de Microelectrónica, Bellaterra, Spain
⁴Lear Automotive EEDS, Valls, Spain

A Comparison of 0.35-micron CMOS Dual-Modulus Prescaler Architectures for ISM 868 MHz

Alfonso Carrera and Frank Oehler
Fraunhofer Institute für Integrierte Schaltungen, Erlangen, Germany

13:10 – **Lunch**