This chapter develops the fundamental models necessary to analyze the essential requirements of switch mode power supplies (SMPSs) as noted in Chapter 2. The large signal continuous and discontinuous mode models for the buck and the boost converters are developed. Then the continuous and discontinuous mode models are integrated into a single unified model for each of the buck and boost converters. The unified buck–boost (conventional flyback converter) and Cuk converter models are next developed. After the development of these models, an example analysis is provided to illustrate the ease and simplicity that this approach affords in analyzing the performance of SMPSs.

3.1 Buck and Boost Converter Continuous Mode Large Signal Models

When a switch mode power converter is modeled, an electrical circuit equivalent model of the duty ratio controller must be created when the converter operates in the continuous mode. From Middlebrook and Cuk, an ideal (AC and DC) transformer equivalent model is conceived and shown in Figure 3.1. The flyback and Cuk converter continuous mode models are in essence cascaded versions of the buck and boost converters and will be dealt with later.

Converting the ideal transformers to a system of dependent generators makes the models more adaptable to most circuit simulation software. Figure 3.2 shows a SPICE model equivalent. The power converter large signal continuous mode models are thus implemented in Figure 3.3. See Cuk and Middlebrook for more information.
3.2 Buck and Boost Converter Discontinuous Mode
Large Signal Models

Now consider the discontinuous mode of operation. From Figure 3.4, the average discontinuous mode inductor current, \( i_{LD} \), is expressed by:

\[
i_{LD} = \frac{I_p}{2} (d + d_2)
\]  

(3.1)

FIGURE 3.2
Ideal transformer equivalent model.
For the buck converter,

\[ I_p = \frac{(v_\text{s} - v)dT_s}{L} \]  \hspace{1cm} (3.2)

**FIGURE 3.4**
Discontinuous mode inductor current.
Also, for periodic volt-second balance across the inductor,

\[ d(v_g - v) = d_2v \]

or

\[ d_2 = d \left( \frac{v_g - v}{v} \right) \]  \hspace{1cm} (3.3)

Substituting Equation 3.2 and Equation 3.3 into Equation 3.1 yields the desired control equation for the buck converter, \( i_{LD} \):

\[ i_{LD} = d^2 \frac{v_g (v - v_g)}{v} \frac{T_s}{2L} \]  \hspace{1cm} (3.4)

For the boost converter,

\[ I_p = \frac{v_g d T_s}{L} \]  \hspace{1cm} (3.5)

and for volt-second balance

\[ dv_g = d_2(v - v_g) \]

\[ d_2 = d \left( \frac{v_g}{v - v_g} \right) \]  \hspace{1cm} (3.6)

Substituting Equation 3.5 and Equation 3.6 into Equation 3.1 yields the control equation for the boost converter, \( i_{LD}' \):

\[ i_{LD}' = d^2 \left( \frac{v v_g}{v - v_g} \right) \frac{T_s}{2L} \]  \hspace{1cm} (3.7)

The next step is to develop a large signal discontinuous mode model from the previous equations. Figure 3.5 shows buck and boost topologies.

The terms \( i_{LD} \) and \( i_{LD}' \) are as yet undefined. With the inductor current starting and returning to zero during each cycle, there is no cyclical energy storage in the inductor. Its properties as an inductive circuit element are nonexistent at the lower frequencies; therefore it does not appear in the models.
With this knowledge, the instantaneous or cyclical power into the converter is equal to the instantaneous power out.

\[ p_{in} = p_{out} \]  \hspace{1cm} (3.8)

For the buck converter,

\[ p_{in} = v_s i_{LD} \]  \hspace{1cm} (3.9)

\[ p_{out} = v_i_{LD} \]  \hspace{1cm} (3.10)

and

\[ i_{LD} = \frac{v}{v_s} i_{LD} \]  \hspace{1cm} (3.11)

For the boost converter,

\[ p_{in} = v_s i_{LD} \]  \hspace{1cm} (3.12)

\[ p_{out} = vi_{LOD} \]  \hspace{1cm} (3.13)
Current $i_{LOD}$ is the correct output current for the boost converter. $i_{LOD}$ is the correct input current for the buck converter and $i_{LOD}$ is the correct output current for the boost converter.

### 3.3 Buck and Boost Continuous and Discontinuous Mode Unified Models

Now combine the continuous and discontinuous mode models into one encompassing unified model, which will emulate an actual converter going from one conduction mode to the other as the critical inductor current boundary is traversed. The schemes depicted in Figure 3.6 and Figure 3.7 provide a simple and straightforward way of implementing this model. A detailed explanation of this topology is now in order. For the moment, ignore the center components of Figure 3.6 consisting of VM2, D1, D2, $i_{LID}$, and F1. The discontinuous mode current, $i_{LD}$, is calculated for all prevailing conditions of $d$, $v_g$, and $v$ according to Equation 3.4. If the voltage, $E$, is sufficiently high to produce an inductor current larger than the value of $i_{LD}$, diode D3 will then conduct. (Diode D3 is modeled as an ideal diode with a forward voltage drop near 0 V. Section 3.10 discusses this further.) The converter is thus in the continuous mode with $i_L > i_{LD}$. D3 basically shorts out current source $i_{LD}$ thus making it appear as though it is not in the circuit.

![Figure 3.6](image-url)

**Figure 3.6**

Buck converter combined continuous and discontinuous mode model.
This is appropriate because $i_{LD}$ is a nonexistent fictitious quantity for $i_L$ greater than any computed quantity greater than $i_{LD}$. If circuit conditions change to lower $i_L$ so that $i_L$ wants to be less than $i_{LD}$, $D_3$ will be reversed biased and the actual inductor current will be $i_{LD}$. The converter is now in the discontinuous mode with $i_L = i_{LD}$.

Now consider the role of the components $VM_2$, $D_1$, $D_2$, $i_{LID}$, and $F_1$ that were ignored earlier. The circuit made from these components is necessary to provide the proper input current that is seen as a load on the power source $v_g$. The circuit is basically a current ORing circuit, with current $i_b$ equal to the larger of the two currents $F_1$ or $i_{LID}$. For example, if current $F_1$ is larger than $i_{LID}$, nonideal diode $D_1$ will conduct, effectively shorting out $i_{LID}$, and $D_2$ is reversed biased with $i_b = F_1$. This is the continuous mode case with $F_2 = i_b = F_1 = d \times i_L$, which is the correct converter input current in the continuous mode. If current $F_1$ decreases below the computed discontinuous mode current, $i_{LID}$, then $i_b$ will be equal to $i_{LID}$, which is the correct discontinuous mode current.

Voltage source $VM_2$ is shown in Figure 3.6 as 1 V, but may be any arbitrary positive value. When a value greater than zero is used for $VM_2$, the voltage at the cathode side of diode $D_2$ will have basically one of two values, depending on the converter conduction mode. This circuit may now also be viewed as a conduction mode detector circuit when monitoring the voltage at the $D_2$ cathode.

Thus, the complete unified continuous and discontinuous mode model for the buck converter is shown in Figure 3.6. It can be recognized from Figure 3.3 and Figure 3.5 that the buck and boost topologies are in essence the duals of each other; therefore, it can be easily deduced that the model shown in Figure 3.7 is the correct unified model for the boost topology by applying the corresponding line of development as for the buck converter.
3.4 Buck–Boost (Flyback) Converter Continuous Mode Large Signal Model

The buck–boost converter is in essence a cascaded combination of the buck and boost converters (Figure 3.1a and Figure 3.1b, respectively). Figure 3.8 shows an equivalent representation of this combination. (See Cuk and Middlebrook for more detail on this.) Replacing the duty ratio controlling switches with their equivalent circuit models as developed in Section 3.1, the equivalent continuous mode model is shown in Figure 3.9.

3.5 Buck–Boost (Flyback) Converter Discontinuous Mode Large Signal Model

From the inductor current waveform of Figure 3.4, Equation 3.1, and the following equations, the average discontinuous mode current, $i_{LD}$, is determined from Figure 3.8.

$$I_p = \frac{v_i d T_s}{L} \quad (3.15)$$
Also,

\[ dv_g = d_2 v \]

or

\[ d_2 = \frac{v_g}{v} \]  \hspace{1cm} (3.16)

Substituting Equation 3.15 and Equation 3.16 into Equation 3.1 yields the desired control equation for the flyback converter:

\[ i_{LD} = d^2 v_g \left( 1 + \frac{v_g}{v} \right) \frac{T_e}{2L} \]  \hspace{1cm} (3.17)

When the flyback converter is modeled only in the discontinuous mode, the average inductor current, \( i_{LD} \), as indicated in Equation 3.17 is not essential, as shown in Figure 3.10. However, its necessity will be noted when developing the unified model. The equations for \( i_{LD} \) and \( i_{LOD} \) are easily noted from Figure 3.4 and Equation 3.15 and Equation 3.16.

\[ i_{LD} = \frac{I_P}{2} d \]

\[ i_{LD} = d^2 v_g \frac{T_e}{2L} \]  \hspace{1cm} (3.18)

and

\[ i_{LOD} = \frac{I_P}{2} d_2 \]

\[ i_{LOD} = d^2 \left( \frac{v_g^2}{v} \right) \frac{T_e}{2L} \]  \hspace{1cm} (3.19)

**FIGURE 3.10**

Flyback discontinuous mode model.
FIGURE 3.11
Flyback converter continuous and discontinuous mode model.
3.6 Buck–Boost Continuous and Discontinuous Mode Unified Model

Following the same unification procedure as that described in Section 3.3, the basic flyback unified model is shown in Figure 3.11. Note the necessity of including $i_{LD}$ here, although it was unnecessary when the discontinuous mode model was considered alone.

3.7 Cuk Converter Continuous Mode Large Signal Model

The continuous mode Cuk converter is in essence a cascaded combination of the boost and buck converters shown in Figure 3.1b and Figure 3.1a, respectively. This is true for the continuous mode, but not necessarily true for the discontinuous mode. Figure 3.12 shows the equivalent representation of this combination. (See Cuk and Middlebrook⁴ for more details on this.) Shown in Figure 3.12 is the noninverting equivalent of the classical Cuk converter (Figure 1.8).

It is interesting to note from Cuk⁶ that the inductor currents $i_{L1}$ and $i_{L2}$ are simultaneously both continuous or both discontinuous and that in the general case these currents do not individually become zero for the discontinuous part of their cycles, but rather the sum of $i_{L1}$ and $i_{L2}$ becomes zero at this point of discontinuity (see Figure 3.14). Replacing the duty ratio controllers with their equivalent circuit models as developed in Section 3.1, the equivalent continuous mode model is shown in Figure 3.13. The output part of the model may be inverted if desired to reflect the more classical negative output.

FIGURE 3.12
Basic boost–buck (Cuk) continuous mode topology.
3.8 Cuk Converter Discontinuous Mode Large Signal Model

From the inductor current waveforms of Figure 3.14 and the following equations, the average discontinuous mode inductor currents $i_{L1D}$ and $i_{L2D}$ are determined from the circuit of Figure 3.12:

$$i_{L1D} = \frac{I_{P1}}{2} (d + d_2) + i$$

(3.20)
where

\[ I_{p1} = \frac{v_s d T_s}{L_1} \]  
\[ I_{p2} = \frac{v d_s T_s}{L_2} \]

For cyclical volt-second balance across \( L_1 \) and \( L_2 \),

\[ d v_s = d_s (v_c - v_g) \]

and

\[ d_s v = d (v_i - v) \]

Eliminating \( v_c \) from Equation 3.24 and Equation 3.25 yields

\[ d_s = \frac{d v_s}{v} \]

Now, combining Equation 3.20 through Equation 3.26 yields

\[ i_{11D} = v_s d^2 \left( 1 + \frac{v_s}{v} \right) \frac{T_s}{2L_1} + i \]

and

\[ i_{12D} = v_s d^2 \left( 1 + \frac{v_s}{v} \right) \frac{T_s}{2L_2} - i \]

From Cuk and Middlebrook,\(^3\)

\[ i = i_{12D} \frac{v_s}{L_1 - L_2} \frac{L_1}{L_1 + L_2} \]
and with cyclical input power equal to cyclical output power,

\[ i_{L2D} = i_{L1D} \frac{v_g}{v} \]  \hspace{1cm} (3.30)

and

\[ i = i_{L1D} \left( \frac{L_1 - \frac{v_g}{v} L_2}{L_1 + L_2} \right) \]  \hspace{1cm} (3.31)

Substituting Equation 3.31 into Equation 3.25 and solving for \( i_{L1D} \) yields

\[ i_{L1D} = v_g d^2 \frac{T_s}{2L_c} \]  \hspace{1cm} (3.32)

where

\[ L_c = \frac{L_1 L_2}{L_1 + L_2} \]

The discontinuous mode noninverting Cuk converter model is then simply shown in Figure 3.15 with \( i_{L1D} \) indicated by Equation 3.32 and \( i_{L2D} \) indicated by Equation 3.30.

### 3.9 Cuk Converter Continuous and Discontinuous Mode Unified Model

Again, following the same unification procedure as described in Section 3.3, the basic Cuk converter unified model is shown in Figure 3.16. Note that the output stage may be inverted for a positive or a negative output.
FIGURE 3.16
Cuk converter continuous and discontinuous mode model.
3.10 Boost Converter Model Analysis Example

Now create a model of a boost converter as an example to illustrate the ease and simplicity of the technique. Consider the duty ratio controlled boost converter of Figure 3.17 operating in the constant frequency mode of 75 kHz (a period of $T_s = 13.33$ µsec).

An equivalent unified PSPICE model is derived from Figure 3.7 and shown in Figure 3.18. The diode, DIDEAL, is modeled as an ideal diode with the characteristics shown in Figure 3.19. This ideal diode model uses $V_F = -1$ µV as opposed to a desired value of zero because, in some applications, a zero value could be divided into other factors, thus causing the simulation to crash. This model does not allow this situation and $V_F$ is small enough that the diode is considered ideal. The ideal diode is here simply generated by a dependent voltage generator and a table function. (See the circuit netlists in Figure 3.22 and Figure 3.23.) In later chapters, netlists will show other ways of creating this ideal diode. If a simulation convergence problem exists, trying a different type of model creation may sometimes help.

The equations for $i_{LD}$ and $i_{LOD}$ are obtained from Equation 3.7 and Equation 3.14, respectively.

$$i_{LD} = 0.017d^2 \left( \frac{v}{v_g} - 1 \right) \quad (3.33)$$
Care must be taken in this simulation that \( v \) does not drop below \( v_g \) because a division by zero may result in Equation 3.33 and cause the simulation to crash. Although not used here, a LIMIT function may be used in the model equation for GILD to prevent this if convergence trouble is encountered. (See the netlists in Figure 3.22 and Figure 3.23).

The steady state critical inductor current (average inductor current at the boundary between the continuous and discontinuous modes of operation)
Three tests will be conducted on the model to reveal some of its characteristics. The first will show the AC response from the duty controller, $d$, to the output voltage, $v$, with the converter operating in the continuous mode ($R < R_{CRIT}$) for $R = 75 \ \Omega$. Then, for the second test, the load resistor will be increased from 75 to 825 \ \Omega, placing the converter in the deep discontinuous mode and examining the AC response under that condition. The third test will be to examine the effect on output voltage of a transient load current.
pulse on the converter forcing it to move from the discontinuous mode ($R = 825\, \Omega$) to the continuous mode and back again with a load current pulse of 0.3 A lasting for 5 msec.

The results of these tests are shown in Figure 3.20 and Figure 3.21. Note the characteristic right-half plane zero for the continuous mode in Figure 3.20. Note that the discontinuous mode AC response of Figure 3.20 is of considerably lower bandwidth with a single pole roll-off and also the absence of

![Graphs showing AC analysis and load transient analysis for a boost converter](image)

**FIGURE 3.20**
Boost converter AC analysis example.

**FIGURE 3.21**
Boost converter load transient analysis example.
Now observe the results of the load transient test in Figure 3.21. Note that the predictable large signal result of the output voltage, \( v \), varies considerably when the inductor current is less than its critical value of 0.106 A. Also note the expected underdamped ringing around the continuous mode output voltage value of 25 V.

Numerous other tests — possibly more practical ones — could be easily devised and conducted on the model to examine easily any large signal transient or small AC characteristic desired. For reference, the PSpice™ netlists for the AC and transient analysis are shown in Figure 3.22 and Figure 3.23, respectively.

**FIGURE 3.22**
Boost converter AC analysis example netlist.

---

Boost Converter AC Analysis
VGDC 8 0 DC 11.25
VGAC 7 8 AC 0
L 7 6 390U
GILD 6 5 VALUE = \((0.017)*PWR(-V(10),2)\)*(V(1)/(V(1)/V(7)-1))
XD1 6 5 DIDEAL
* 'Ideal Diode Model
.SUBCKT DIDEAL 1 2
EID 3 1 TABLE [V(3,2)] = (-1,1U)(0,1U)(1,1)
DIO 3 2 D
.ENDS
* E 5 4 VALUE = [V(11)]*V(1)
VM 4 0 DC 0
G 0 3 VALUE = [V(11)]*I(VM1)
GILOD 3 2 VALUE = [V(7)/V(0)]*I(VM1)
D 1 0 3 D
D 2 3 2 D
VM 2 0 DC 0
F 2 0 VM 2 1
C 1 0 24U
* .PARAM RVAL = 1
ROUT 1 0 [RVAL]
.STEP PARAM RVAL 75 825 750
*
VD 1 1 10 DC 1
VDCC 9 10 DC .55
VDAC 0 9 AC 1
RD 1 1 0 1K
*
.MODEL D D IS = 1N
.AC DEC 40 100 100K
.PROBE
.END
Fundamental Switch Mode Converter Model Development

3.11 Summary

This chapter has developed the fundamental conceptual computer models for the four major pulse width modulated (PWM) power converter topologies. Many unique converter topologies exist, but in most instances they can be reduced to one in these four major categories. These models accept input power, \( v_i \), and PWM control, \( d \), to provide output voltage, \( v_o \), with the controlling variable, \( d \), controlled directly by some control signal. The converters, as depicted, are commonly known as “voltage mode” or “duty
ratio-controlled” converters. These models may be used directly as shown in this chapter to obtain first-order analysis results for single output voltage SMPSs. In subsequent chapters, these models will be embedded within other control schemes to allow for current mode control analysis along with more practical expansions. These include multiple outputs and macromodels of commercially available PWM integrated circuit controllers.