A Novel Technique to Compensate Voltage Sags in Multiline Distribution System—The Interline Dynamic Voltage Restorer

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Abstract—The dynamic voltage restorer (DVR) provides a technically advanced and economical solution to voltage-sag problem. As the voltage-restoration process involves real-power injection into the distribution system, the capability of a particular DVR topology, especially for compensating long-duration voltage sags, depends on the energy storage capacity of the DVR. The interline DVR (IDVR) proposed in this paper provides a way to replenish dc-link energy storage dynamically. The IDVR consists of several DVRs connected to different distribution feeders in the power system. The DVRs in the IDVR system share a common energy storage. When one of the DVRs compensates for voltage sag appearing in that feeder, the other DVRs replenish the energy in the common dc-link dynamically. Thus, one DVR in the IDVR system works in voltage-sag compensation mode while the other DVRs in the IDVR system operate in power-flow control mode. In principle, IDVR can operate effectively when constituent DVRs are electrically (not necessarily physically) far apart. Closed-loop load voltage and current-mode-control techniques are used as the control strategy in the two modes of operation. Experimental results obtained for a laboratory prototype of the IDVR are presented to show the effectiveness and the efficacy of the proposed IDVR system to improve power quality.

Index Terms—Current-mode control, dynamic voltage restorer (DVR), interline dynamic voltage restoration, phase advance, power quality.

I. INTRODUCTION

With the widespread use of electronic equipment, loads are becoming more sensitive and less tolerant to short-term voltage disturbances in the form of voltage sags. Custom power is a technology-driven product and service solution which embraces a family of devices to provide power-quality enhancement functions. Among the several novel custom-power devices, the dynamic voltage restorer (DVR) [1], [2] is the most technically advanced and economical device for voltage-sag mitigation in distribution systems. The conventional DVR [2] functions by injecting ac voltages in series with the incoming three-phase network, the purpose of which is to improve voltage quality by adjustment in voltage magnitude, wave shape, and phase shift. These attributes of the load voltage are very important as they can affect the performance of the protected load. The voltage-sag compensation involves injection of real and reactive power to the distribution system, and this determines the capacity of the energy storage device required in the restoration scheme. The reactive power requirement can be generated electronically within the voltage source inverter of the DVR. An external energy storage is necessary to meet the real-power requirement. Thus, the maximum amount of real power that can be supplied to the load during voltage-sag compensation is a deciding factor of the capability of a DVR, especially for mitigating long-duration voltage sags. Voltage injection with an appropriate phase advance with respect to source side voltage can reduce the energy consumption [2]. However, the energy requirement cannot be met by the application of such phase-advance technique alone for mitigating deep sag of long duration, as it is merely a way of optimizing existing energy storage. If the dc link of the DVR can be replenished dynamically by some means, the DVR will be capable of mitigating deep sags with long durations.

The interline IDVR (IDVR) proposed in this paper provides a way to replenish the energy in the common dc-link energy storage dynamically. The IDVR system consists of several DVRs protecting sensitive loads in different distribution feeders emanating from different grid substations, and these DVRs share a common dc link. The interline power-flow controller (IPFC) proposed in [3] addresses the problem of compensating a number of transmission lines at a given substation. The IPFC scheme provides a capability to transfer real power directly between the compensated lines, while the reactive power is controllable within each individual line. The IDVR scheme provides a way to transfer real power between sensitive loads in individual line through the common dc link of the DVRs, as it does in the IPFC. However, the lines in the IPFC originate from a single grid substation while the lines in the IDVR system originate from different grid substations. When one of the DVRs in IDVR system compensates for voltage sag by importing real power from the dc link, the other DVRs replenish the dc-link energy to maintain the dc-link voltage at a specific level. An example of a potential location for such a scheme is an industrial park where power is fed from different feeders connected to different grid substations, those that are electrically far apart. The sensitive loads in this park may be protected by DVRs connected to respective loads. The dc links of these DVRs can be connected to a common terminal, thereby...
forming an IDVR system. This would cut down the cost of the custom-power device, as sharing common dc link reduces the size of the dc-link storage capacity substantially, compared to that of a system in which loads are protected by clusters of DVRs with separate energy storage systems.

The control system of a DVR plays an important role, with the requirements of fast response in the face of voltage sags and variations in the connected load. Generally, there are two control schemes, open loop [4] and closed loop [5], which are used in the DVR applications. This paper presents an extensive analysis to develop suitable control strategies for the DVRs in the IDVR scheme. The proposed IDVR control system consists of a closed-loop load voltage and current-mode controller for the individual DVR.

II. OPERATION OF IDVR

The IDVR system consists of several DVRs in different feeders, sharing a common dc link. A two-line IDVR system shown in Fig. 1 employs two DVRs connected to two different feeders originating from two grid substations. These two feeders could be of the same or different voltage level. When one of the DVRs compensates for voltage sag, the other DVR in IDVR system operates in power-flow control mode to replenish dc-link energy storage which is depleted due to the real power taken by the DVR working in the voltage-sag compensation mode. Propagation of voltage sags due to fault in the power system depends on many factors, such as voltage level, fault current, transformer in the propagation path and their connection arrangement, etc. Voltage sags in a transmission system are likely to propagate to larger electrical distance than that in a distribution system. Due to these factors and as the two feeders of the IDVR system in Fig. 1 are connected to two different grid substations, it is reasonable to assume that the voltage sag in Feeder 1 would have a lesser impact on Feeder 2. Therefore, the upstream generation-transmission system to the two feeders can be considered as two independent sources. These two sources are represented by the Thevenin’s equivalent voltage sources $V_{s1}$ and $V_{s2}$ in series with Thevenin’s equivalent impedances $Z_{t1}$ and $Z_{t2}$ connected to the buses B1 and B2 as in Fig. 1. $Z_{l1}$ and $Z_{l2}$ are calculated based on the fault level at $B_1$ and $B_2$.

![Schematic diagram of an IDVR in a two-feeder system.](image1)

III. POWER-FLOW ANALYSIS OF IDVR SYSTEM

Consider the condition when one of the DVRs in the IDVR system operates in voltage-sag compensating mode while the other DVRs operate in power-flow control mode to keep the dc-link voltage at a desired level. To set up power-flow analysis of the two-feeder IDVR system shown in Fig. 1, it is assumed that DVR1 in Feeder 1 operates in the voltage-sag compensation mode and DVR2 in Feeder 2 works in the power-flow control mode. When there is no voltage sag, the load voltage of Feeder 2 is equal to the bus voltage $V_{b2}$. Even in sag situations, the DVR2 should be operated to meet this condition while supplying real power to the common dc link. Hence, the locus of the $V_{b2}$ should lie on a circle with radius equal to the desired magnitude of bus voltage $V_{b2}$, as shown in Fig. 2. The load voltage ($V_{l2}$) has an advance phase angle $\beta$ with respect to the supply side voltage ($V_{b2}$), in order to inject power to the dc link. With the help of a phasor diagram in Fig. 2, the following expression can be derived for the real power exchange between the two feeders:

$$P_{ex} = S_{l2} \left[ \cos(\phi_2 - \beta) - \cos(\phi_2) \right]$$

where $S_{l2} = 3V_{l2}I_{l2}$ is Feeder 2 load apparent power, $V_{l2}$, $I_{l2}$, and $\phi_2$ are the Feeder 2 load voltage, current, and power-factor angle.

According to (1), the real-power exchange depends on the advance angle $\beta$, as the other parameters of (1) are constant for a given loading condition. Therefore, the maximum real power transfer is reached when $\beta$ is advanced, such that, it is equal to the load power-factor angle (i.e., $\beta = \phi_2$). In this condition, the supply side voltage is in phase with the Feeder 2 current. Thus, the maximum real power is given by (2)

$$P_{ex, max} = S_{l2}[1 - pf^2]$$

where $\beta_{max} = \phi_2$ and $pf^2 = \cos(\phi_2)$ is Feeder 2 load power factor. According to (2), the maximum value of the real-power transfer from the Feeder 2 to Load 1 is 20% of base load VA rating of Load 2 for a typical load power factor of 0.8. This amount of extra power can be transferred from Feeder 2 to Load 1 without stressing the feeder in short run.

![Phasor diagram of DVR2 for real-power transfer.](image2)
The real power exchange can also be expressed in terms of the real power imported by DVR1 and the system losses including converter switching losses, as follows:

\[ P_{\text{ex}} = P_{\text{DVR1}} + P_{\text{losses}}. \]  

Then, \( \beta \) can be expressed as

\[ \beta = \phi_2 - \cos^{-1} \left[ \frac{P_{\text{DVR1}} + P_{\text{losses}}}{S_{l2}} \right]. \]  

According to (4), \( \beta \) mainly depends on the real power taken by DVR1. The real power injected by DVR1 to compensate a particular sag is decided by the type of voltage-restoration method, such as in-phase injection [4], presag-supply-voltage injection [4], and energy-saving injection [2], [6]. When the voltage sag contains a phase-angle jump, the in-phase-injection technique introduces the same phase-angle jump to the load, which is not desirable. If the voltage sag does not contain a phase-angle jump, the in-phase-injection method is similar to the presag-supply-voltage injection. Therefore, the real-power requirement in the presag supply voltage and energy-saving injection methods is addressed in the following sections.

A. DVR1 Operating in Presag-Supply-Voltage Injection

One commonly used voltage-injection method for DVR is to compensate for the difference between the sag and presag voltages. Even though this method gives an undisturbed restored voltage, it requires a sufficiently large energy storage and voltage-injection capability. Fig. 3 depicts the phasor-diagram representation of this restoration method. Under this method, the real-power transfer from DVR1 to the load is given as

\[ P_{\text{DVR1pr}} = S_{l1} \left[ \text{pf1} - \frac{R}{3} \cos(\phi_1 + \theta) \right]. \]  

where the term \( R = \sqrt{X^2 + Y^2} \) with \( X = \sum_{j=1}^{3} a_j \cos(\delta_j) \), \( Y = \sum_{j=1}^{3} a_j \sin(\delta_j) \), and \( \theta = \tan^{-1}[Y/X] \). The sag factor \( a_j = V_{b1j}/V_{l1j} \) and \( V_{l1j} \) is the Feeder 1 load voltage. \( \delta_j \) is the phase shift of the supply voltage \( V_{b1j} \), \( \phi_1 \) is the Feeder 1 load power-factor angle, and \( S_{l1} \) is the apparent power of the load in Feeder 1.

Assuming a balanced voltage sag with sag factor \( a \) and phase-angle jump \( \delta \), from (4) and (5), \( \beta \) can be expressed as follows:

\[ \beta = \phi_2 - \cos^{-1} \left[ \frac{S_{l1} \left[ \text{pf1} - a \cos(\delta + \phi_1) \right] + P_{\text{losses}}}{S_{l2}} \right]. \]

Thus, for maximum real-power transfer

\[ a = \frac{\left[ S_{l1} \text{pf1} + P_{\text{losses}} - S_{l2}(1 - \text{pf2}) \right]}{S_{l1} \cos(\phi_1 + \delta)}. \]

If there is \( n \) number of feeders in the IDVR system, (7) can be written as (8), shown at the bottom of the page. For example, assume that the two feeders carry equal loads with the same power factors (pf), and the system losses are 3% of the load apparent power. Under this situation, the sag factor can be presented as

\[ a = \frac{[2 + \text{pf} - 0.97]}{\cos(\phi_1 + \delta)}. \]

According to (9), the sag factor \( a \) depends not only on the power factor of the loads but also on the phase jump \( \delta \) of the supply voltage. The variation of \( a \) for different \( \delta \) for a given load power factor is presented in Fig. 4. This plot reveals that the depth of the sag that can be mitigated with the real power provided by the DVR2 reduces with positive \( \delta \). It will increase with negative \( \delta \) before it decreases. However, according to (8), \( a \) can be reduced if the IDVR system consists of large number of feeders. Since \( \delta \) is not controllable, DVR1 operating in presag-supply-voltage boosting technique will generally require a
**B. DVR1 Operating in Energy-Saving Voltage Injection**

Voltage injection with an appropriate phase advance with respect to source side voltage can reduce the consumption of energy, from the perspective of the DVR energy storage [2], [6]. In this technique, the phase-advance angle, which will minimize the consumption of the dc-link energy, is calculated. The angle is progressively advanced with respect to the presag supply voltage. Complete theoretical analysis for a generalized sag situation has been presented in [2] and [6]. The phasor diagram shown in Fig. 5 illustrates the phase-advance technique.

The optimum real power required to mitigate voltage sag can be written in the following equation with \( P_{DVR1} > 0 \)

\[
P_{DVR1opt} = S_{l1} \left[ pf1 - \frac{R}{3} \right]
\]

where \( \alpha_{opt} = \phi_1 + \theta \) and \( \alpha_j, X, Y, \theta, \) and \( R \) are as given in (5).

For a balanced three-phase voltage sag with sag factor \( \alpha \) and phase-angle jump \( \delta \), \( R = 3 \ast \alpha \). Hence, \( \beta \) is given as

\[
\beta = \phi_2 - \cos^{-1} \left[ \frac{S_{l1}[pf1 - \alpha] + P_{\text{losses}}}{S_{l2}} + pf2 \right].
\]

For maximum real power transfer

\[
a = \left[ S_{l1}pf1 + P_{\text{losses}} - S_{l2}(1 - pf2) \right].
\]

Consider the same example of a two-line IDVR system with equal load, power factors (pf), and 3% system power losses with respect to the apparent power of the load. Under this situation, the sag factor is given as

\[
a = [2 \ast pf1 - 0.97].
\]

According to (13), the sag factor is independent of phase-angle jump, unlike the case when using the presag-supply-voltage-injection technique. For a balanced three-phase voltage sag with phase-angle jump \( \delta \), the optimum phase advance (\( \alpha_{opt} \)) is the summation of load power-factor angle (\( \phi_1 \)) and the supply-voltage phase-angle jump (\( \delta \)). Therefore, the supply voltage is in phase with the feeder current (same as the load current). Therefore, the real power given by the supply source is independent of the phase-angle jump under the energy saving voltage-restoration method. This is another distinguished advantage of the energy-saving voltage-restoration method over the presag-supply-voltage-restoration method. For a 0.8 power-factor load, the real-power support given by DVR2 can be used to mitigate long-duration voltage sag of up to about 37%, which appears in Feeder 1. Therefore, it is desirable to operate DVR1 of IDVR system in energy-saving voltage injection mode.

**IV. CONTROL SYSTEM FOR THE DVR1 IN VOLTAGE INJECTION MODE**

The DVR output voltage depends on the accuracy and dynamic behavior of the pulsewidth-modulated (PWM) synthesis scheme and the control system used. Usually, the control voltage of the DVR is derived by comparing the incoming supply voltage against a desired reference voltage [4]. Although system stability is guaranteed in this type of control, damping is poor, and the stability margin may not be sufficient in the presence of inverter-side filter [5]. Poor damping results in sustained voltage oscillations in the distribution network, which could have serious adverse effects on sensitive loads and equipment such as adjustable speed drives. The drawbacks of the open loop control system can be avoided with multiloop feedback control system where a voltage loop is incorporated externally to an inner current loop taken from the filter capacitor current of the DVR [5]. Fig. 6 depicts a detailed schematic diagram of DVR1 in the two-feeder IDVR system. With reference to Fig. 6, the following expressions can be derived to model DVR1

\[
V_{i1} = V_{c1} + (r_i + s_l)i_{i1}
\]

\[
i_{i1} = i_{c1} + n_i i_{l1}
\]

\[
i_{c1} = C_i s V_{c1}
\]

\[
V_{\text{inj1}} = n V_{c1} - n^2(r_i + s_l)i_{l1}
\]

\[
V_{l1} = V_{l0} + V_{\text{inj1}}.
\]

Using the set of expressions in (14) for DVR1, multiloop current mode voltage regulator for controlling DVR1 output voltage is developed as shown in Fig. 7. The load voltage is compared with its reference value, and the error is multiplied with the voltage gain \( k_v \) to get a virtual-capacitor-current reference. This virtual capacitor current is compared with the measured capacitor current, and the result is multiplied by
the current gain $k_c$. The resulting quantity is then added with feedforward voltage to derive the control signal for the PWM generator of the inverter.

### A. Control System Analysis

The DVR1 begins its operation at the instant of voltage sag appearing in Feeder 1. The initial power drawn from the dc-link capacitor as DVR2, which operates in power-flow control mode, would need a little time to react to the real-power demand of DVR1. Therefore, the dc-link capacitors are sized to provide this initial power. In the presence of semiconductor switches in the inverter bridge, the DVR inverter model is nonlinear. However, it is possible to describe the DVR behavior in differential or difference form using the state space averaging technique. Therefore, the inverter of the DVR is modeled as a linear amplifier with a constant gain $k_i$ as shown in Fig. 7. The sensitive load protected by the DVR can vary from linear to nonlinear time invariant to nonlinear time-varying type. In view of this complexity, a linear constant impedance load is assumed, and the controller gains are selected, such that, the controller is robust for the load model uncertainty.

The load voltage of the controller shown in Fig. 7 can be written as

$$V_{l1} = G_{vref}V_{ref} + G_{vbl}V_{bl}$$

where $G_{vref} = nk_i(k_t + k_vk_v)(r_t + sl_t)/(a_3s^3 + a_2s^2 + a_1s + a_0)$, $G_{vbl} = (b_3s^3 + b_2s^2 + b_1s + b_0)/(a_3s^3 + a_2s^2 + a_1s + a_0)$, and $a_j$ and $b_j$ are given in Appendix I.

The system characteristic equation is a third-order polynomial and has one real root and two complex conjugate poles. Thus, the characteristic equation can be factorized as

$$CE \cong C_{l1} \left[ (l_t + n^2l_t)s + (r_t + n^2r_t) \right] \left[ s^2 + c_1s + c_0 \right]$$

where $c_1$ and $c_0$ are also given in Appendix I.

In view of voltage regulation at the load terminal, $l_t \gg n^2l_t$ and $r_t \gg n^2r_t$. Then, substituting for denominator of $G_{vref}$ from (16), the following expression is obtained:

$$G_{vref} \approx \frac{nk_i(k_t + k_vk_v)(r_t + sl_t)}{C_{l1}(r_t + sl_t)[s^2 + c_1s + c_0]}$$

$$= \frac{nk_i(k_t + k_vk_v)}{C_{l1}[s^2 + c_1s + c_0]}.$$  \hspace{1cm} (17)

The real root of the characteristic equation expressed in (16) is approximately located at $-r_t/l_t$, and it cancels out with the zero of $G_{vref}$ as given in (17). Therefore, the other two complex conjugate poles of (17) mainly govern the dynamic properties of the closed-loop control system. The steady-state error ($\epsilon_{ss}$) for a sinusoidal input and the system damping ratio ($\xi$) are expressed by (18). The gain parameters $k_i$ and $k_c$ of the controller can be determined using these two equations to satisfy the given design specification of the DVR controller. The feedforward gain of the controller does not contribute for system damping and stability, as it is present only in the numerator of the transfer functions. However, this gain $k_i$ can be adjusted to reduce the steady-state error of the system.

$$\epsilon_{ss} = \left[ 1 - \frac{nk_i(k_t + k_vk_v)\sqrt{r_t^2 + w_0^2l_t^2}}{\sqrt{(a_0 - a_2w_0^2)^2 + w_0^2(a_1 - a_3w_0^2)^2}} \right] \times 100$$

$$\xi = \frac{(r_t + k_ck_v)}{2\omega_cn_l}.$$  \hspace{1cm} (18)

In (18), $\omega_c \cong (1/\sqrt{C_{l1}})\sqrt{(1 + nk_i(k_t + k_vk_v))}$ and $w_0$ is the frequency of the supply voltage.

### B. Reference Signal Generation for DVR1 Controller

As stated in Section III-B, it is desirable to adopt the energy-saving technique for DVR1 so that the real power given by DVR2 can be used to mitigate voltage sags with large depth and duration. As the load voltage phase angle ($\alpha$) is progressively advanced in this technique to minimize the energy taken from the dc-link energy storage, $\alpha$ has to be calculated in real time. This requires the detection of the supply voltage magnitude and phase jump. Until the supply voltage parameters are available for calculating $\alpha$, DVR1 is operated in presag-supply-voltage boosting technique.

The supply-voltage-parameter estimation can be carried out using either discrete Fourier transform (DFT) method or Kalman filtering algorithm. However, the DFT and FFT algorithms suffer from certain limitations such as the requirement of input to be stationary and the number of samples per cycle should be an integer number. These limitations can be eliminated by Kalman filtering approach. Theoretical approach
Therefore, the dc-link capacitor should be selected to supply the initial transient energy at the start of DVR1 operation. For current-mode controllers, the initial transient energy at the start bus voltage controller is slower in response compared to the voltage and comparing it with the desired reference. As the dc-link voltage is the device power losses in DVR1 and DVR2.

A. Reference Voltage Generation for DVR2 in Power-Flow Control Mode

Fig. 9 shows the block diagram for generating reference voltage for DVR2 to operate in power-flow control mode. The load voltage advance angle (\( \beta \)) is calculated by deriving a reference active supply current (\( i_d^* \)) which depends on the dc bus voltage regulator instantaneous real power. Referring to Fig. 9, the dc-link voltage error is regulated through a PI controller to obtain the real-power flow (\( P_{\text{ex}} \)) to the dc-link from Feeder 2. \( P_{\text{ex}} \) is added to the real-power reference (\( P_{2\text{ref}} \)) of the load of Feeder 2 to determine the total power supplied by the Feeder 2. Then, the desired current component that governs the real-power flow in Feeder 2, \( i_d^* \), can be calculated from the first expression given in (20) where \( V_{2d} \) is obtained by transforming three-phase supply voltage (\( V_{2} \)) to a synchronously rotating reference frame dq0-axes, where \( d \)-axis is aligned with the vector of \( V_{2} \) as shown in Fig. 10. As the magnitude of the load voltage (\( V_{2} \)) is fixed to magnitude of \( V_{2d} \), the reference voltage \( V_{2\text{ref}} \) for the power-flow controller can easily be calculated.

With reference to Figs. 9 and 10, the following set of expressions can be derived:

\[
\begin{align*}
\beta &= \phi_2 - \cos^{-1}\left(\frac{i_d^*}{i_{2m}}\right) \\
V_{2d} &= V_{12m} \cos(\beta) \\
V_{2q} &= V_{12m} \sin(\beta)
\end{align*}
\] (20)

where \( V_{12m} \) and \( i_{2m} \) are peak values of Feeder 2 load voltage and current, respectively.

VI. EXPERIMENTAL RESULTS

A laboratory prototype of the two-line IDVR system as shown in Fig. 11(a) has been constructed for the experimental verification of the IDVR system performance with the implementation of the control algorithms. The schematic of the hardware system is shown in Fig. 11(b). The parameters of the IDVR prototype used in the experimental setup are given in Appendix II. Two three-phase low-voltage programmable power sources (sag generators) supply power to two \( R-L \) loads of the same power ratings, series connected through the two injection transformers. The primary windings of the transformers are connected to two PWM voltage source inverters (voltage source inverters 1 and 2), which consist of insulated gate bipolar transistor (IGBT) switches through \( LC \) low-pass filters. Implementation of control algorithms for the IDVR system is accomplished via dSPACE DS1103 controller board. Source
Fig. 9. Block diagram representation of reference voltage generation for the power-flow controller.

![Diagram](image_url)

Fig. 10. Representation of \( V_{b_2d}, i_{b_2}, \) and \( V_{b_2} \) in \( d-q \) reference frame.

![Diagram](image_url)

and load voltage as well as filter capacitor currents and common dc-link voltage are measured by transducers, and the measured signals are fed to the A/D converters in the DSP card for real-time control of the IDVR system. A software phase-locked loop (SPLL) which calculates supply voltage parameters and necessary phase angle advance is used to generate the reference for the controller for mitigating voltage sag. The reference for the power-flow controller is obtained by another software program, which implements the reference generation algorithm shown in Fig. 9. The sampling frequency of the control system is set to 8 kHz.

Fig. 12(a) depicts the Feeder 1 supply voltage with an occurrence of a voltage sag of 40% with 200-ms duration. The compensated load voltage shown in Fig. 12(b) accurately follows the reference generated by the SPLL when DVR1 operated under the proposed multiloop feedback control system. It is noted that the degree of damping and dynamic performance of the load voltage has increased significantly compared to the open loop control of DVR1. Fig. 12(c) shows the phase-advance angle \( \alpha \) calculated in real time using the SPLL. This angle is progressively advanced at the beginning of the DVR1 operation, and it has been progressively retarded after the voltage sag. Fig. 12(d) depicts the load voltage of Feeder 2. The load voltage phase angle has been progressively advanced with respect to the supply voltage in order to provide the real power to replenish the dc-link energy. The load voltage accurately tracks the reference generated depending on the real-power requirement. The dc-link voltage shown in Fig. 12(e) indicates an initial drop at the start of DVR1 operation, and the dc-link voltage is maintained at a value slightly below the reference dc-link voltage. The initial power requirement of DVR1 is further aggravated as the initial load voltage of Feeder 1 is in phase with its presag supply voltage. This means that the dc link needs to supply certain amount of additional power until load 1 voltage angle is gradually advanced to bring DVR1 to energy optimum mode. As stated in Section III, Feeder 2 can supply real power to compensate voltage sag of 40% if the losses are assumed to be negligible. However, the copper losses in the laboratory prototype are higher than the IGBT losses due to the resistances in the injection transformers.

![Diagram](image_url)

Fig. 11. (a) Laboratory hardware prototype of the IDVR system. (b) Schematic diagram of IDVR hardware prototype.
and filters. As the sag appears in Feeder 1, the Feeder 2 load voltage is progressively advanced as in Fig. 12(f).

VII. CONCLUSION

This paper proposes the concept of IDVR, which is an economical approach to improve multiline power quality. The IDVR considered in this paper consists of several DVRs which are electrically far apart, connected to a common dc link. When one of the DVRs compensates a voltage sag, the other DVRs are used to replenish the dc-link stored energy. The control scheme for the IDVR includes a multiloop feedback control system, which is identical for both the voltage compensation and the real-power control. The only difference is the way the reference signal is generated, and it depends on the mode of operation. In real-power-flow control mode, the reference is generated according to the real-power requirement demanded by the DVR performing the voltage restoration. The analysis shows that a two-line IDVR system can mitigate about 40% voltage sag with long duration appearing in one of the lines. The experimental results show the efficacy of the proposed IDVR.
TABLE I
PARAMETERS OF THE TWO-LINE IDVR SYSTEM SHOWN IN FIG. 1

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Feeder 1</th>
<th>Feeder 2</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply Voltage (V)</td>
<td>(-V_s)</td>
<td>130</td>
</tr>
<tr>
<td>Load resistance (Ω)</td>
<td>(-r_t)</td>
<td>40.0</td>
</tr>
<tr>
<td>Load inductance (mH)</td>
<td>(-l_t)</td>
<td>95.5</td>
</tr>
<tr>
<td>Transformer resistance (Ω)</td>
<td>(-r_t)</td>
<td>3.0</td>
</tr>
<tr>
<td>Transformer leakage inductance (mH)</td>
<td>(-l_t)</td>
<td>10.0</td>
</tr>
<tr>
<td>Filter resistance (Ω)</td>
<td>(-r_f)</td>
<td>0.4</td>
</tr>
<tr>
<td>Filter inductance (mH)</td>
<td>(-l_f)</td>
<td>5.0</td>
</tr>
<tr>
<td>Transformer capacitance (μF)</td>
<td>(-C_t)</td>
<td>30.0</td>
</tr>
<tr>
<td>Common DC-link Capacitance (μF)</td>
<td></td>
<td>3200</td>
</tr>
<tr>
<td>Common DC-link voltage (V) - (V_{DC})</td>
<td></td>
<td>210</td>
</tr>
</tbody>
</table>

APPENDIX I

\[
\begin{align*}
 a_3 &= C_t l_t (l_t + n^2 l_t) \\
 a_2 &= C_t [r_t l_t + l_t r_t + n^2 r_t l_t + n^2 l_t r_t + k_c k_i l_t + n^2 k_c k_i l_t] \\
 a_1 &= [C_t r_t r_t + n^2 C_t r_t r_t + n^2 l_t + l_t + k_c k_i C_t r_t] \\
 &\quad + n k_c k_i l_t + n^2 l_t + n^2 l_t + n^2 k_c k_i C_t r_t] \\
 a_0 &= n^2 r_t + r_t + n k_c k_v k_i r_t + n^2 r_t \\
 b_3 &= C_t l_t l_t \\
 b_2 &= C_t [r_t l_t + l_t r_t + k_c k_i l_t] \\
 b_1 &= C_t r_t r_t + l_t + k_c k_i C_t r_t - n k_i k_i l_t \\
 b_0 &= r_t (1 - n k_i k_i) \\
 c_1 &= \frac{r_t + k_c k_i}{l_t} \\
 c_0 &= \frac{n^2 (r_t + r_t) + r_t (1 + n k_c k_v k_i)}{C_t l_t (r_t + n^2 r_t)} \\
 &\approx \frac{(1 + n k_c k_v k_i)}{C_t l_t}
\end{align*}
\]

\(C_t\)—filter capacitance, \(l_t\)—filter inductance, \(r_t\)—filter resistance, \(r_t\)—transformer resistance, \(l_t\)—transformer leakage inductance, \(r_t\)—load resistance, \(l_t\)—load inductance, \(n\)—transformer winding ratio,

APPENDIX II

See Table I.

REFERENCES


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