softFM: An all-Digital Stereo FM Transmitter with RDS based on *Software Radio* Architectures

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Abstract

This resume describes the realization of a fully digital stereo FM Transmitter with RDS capability (Radio Data System), based on *software radio* architectures using FPGAs. This system can be remotely controlled by means of a WEB interface.
Keywords: Software radio, Numeric FM, Direct Digital Synthesis, Cauer-Chebyshev filter, FPGA, Verilog HDL

1 Introduction

Nowadays there is a great effort to replace all (or nearly all) the analog components of a communication system by architectures using digital hardware, whose functionality can be software configurable using FPGAs and/or DSPs. Radio communication systems based on these new architectures are generally termed *software radios*.

These kind of radio architecture possesses important advantages when compared to its analog counterparts. The most relevant are:

- substantially better repeatability and stability (component aging and matching are no longer factors of performance limitation);
- implementation of signal processing functions that are unrealizable with analog hardware (for instance, FIR filters);
- hardware "tweaking" replaced by software tuning;
- design of cost-effective multifunction radios supporting different modulation types and bandwidths;
- potential reduction in product cost and development time.

The system that will be presented is an all-digital implementation of a commercial band FM transmitter with stereo and RDS capabilities. This transmitter accepts an S/PDIF digital audio stream as its input and the RF carrier is directly generated and modulated by a very high-speed *direct digital synthesizer* (DDS). All the required signal processing is performed in a medium density FPGA.

2 Direct digital synthesis

DDS technology [1] is an innovative circuit architecture that allows fast and precise manipulation of its output frequency, under full digital control. DDS also enables very high resolution in the incremental selection of output frequency, generating a phase-continuous waveform.

The basic functional block diagram and signal flow of a DDS system is shown in Figure 1.

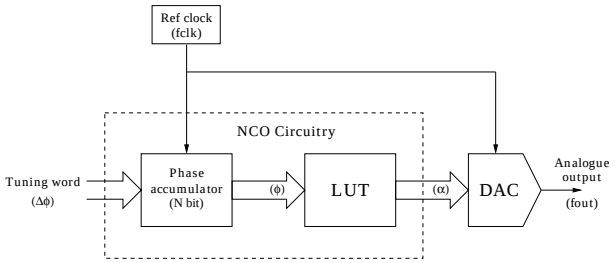


Figure 1: softFM block diagram

The output frequency of a DDS system can be expressed by $f_{out} = \Delta\phi \times f_{clk}/2^N$, usually called *tuning equation,* where $\Delta\phi$ is the phase increment value of the accumulator, f_{clk} is the system clock frequency and N is the accumulator resolution. Being f_{clk} and N fixed system parameters, the output frequency is linearly dependent of the phase increment number.

In analog systems, FM is accomplished by using reactance modulation. Typically, the modulating analog signal is applied to a varicap diode which forms part of the resonant oscillator circuit. Unfortunately the relationship be-

tween modulating voltage and oscillator frequency is nonlinear. Furthermore, it is often difficult to prevent overmodulation and maintain consistent deviations over wide output center frequency variations. All these problems are completely solved with DDS numeric FM. Linearity is typically orders of magnitude better in numeric FM systems than analog reactance modulators [2].

In the last couple of years, there has been a considerable increase in the availability of low-power, high-performance and high-speed DDS devices based on the CMOS fabrication process. As an example, the synthesizer chip used in this transmitter — the AD9852 from Analog Devices [3] — is a 300 MHz DDS with 48-bit of frequency resolution and incorporating a 12-bit D/A converter. This is the state-of-the-art in CMOS DDS components.

3 System description

The global block diagram of the softFM transmitter is depicted in Figure 2.

The following subsections describe in more detail the constituent blocks of this transmitter.

3.1 Digital audio interface

S/PDIF is actually one of the most common digital formats of audio signals and there is a trend for all the audio equipment to have a S/PDIF digital audio input and/or output. The S/PDIF receiver used in this project supports audio sampling rates from 32 kHz to 96 kHz and provides all the synchronization signals needed to to extract the PCM audio samples. The S/PDIF interface board is depicted in Figure 3.

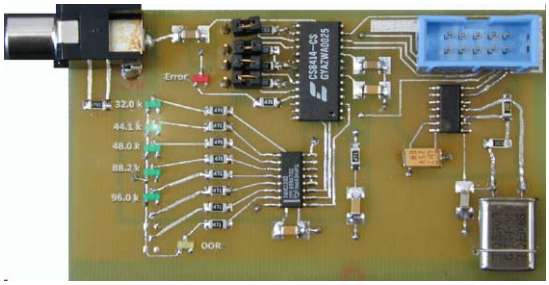


Figure 3: S/PDIF interface board

3.2 Digital signal processing

The entire FM multiplex baseband processing is performed in a XC4010E FPGA from Xilinx [4], with an approximate equivalent capacity of 10 kgates. From the digital audio stream provided by the S/PDIF receiver, the left and the right audio samples are extracted and further processed to generate the composite FM stereo signal (usually referred as the MPX signal). The other task of the FPGA is to add the 57 kHz subcarrier that is modulated by the RDS stream.

The FPGA will be upgraded into a higher density device from the new Spartan-II family, enabling the use of higher internal precision data calculation, the realization of more accurate digital filters and higher speed of operation. Verilog HDL was the language used to implement all signal processing functions.

The prime function of the microcontroller is to generate the RDS stream and configuration parameters to the FPGA. These include carrier frequency and maximum frequency deviation. The RDS data stream is encoded in compliance with the RDS standard [5].To implement this module, the Philips 89C51RD+ microcontroller with built in memory was employed and programmed using the ANSI C language.

3.3 Direct digital synthesizer

The core component of the transmitter is the Analog Devices AD9852 high-performance direct digital synthesizer. The AD9852's high speed DDS core provides a 48-bit frequency tuning word, which results in an output tuning resolution of approximately l μHz for a 300 MHz reference clock input (its maximum operating frequency). The AD9852 also incorporates a built-in programmable reference clock multiplier, enabling the use of such high sampling rates from lower frequency external clock sources. A reference clock of 40 MHz was used. Due to the version of the synthesizer employed (one with a higher thermal impedance package) the internal operating frequency had to be limited to 240 MHz, otherwise the risk of thermal breakdown was considerable (at this frequency the device consumption is approximately 2 W). Even so, a heatsink had to be mounted on top of the device to maintain its temperature at acceptable levels (Figure 4).

As this system uses 240 MHz of internal clock frequency, the carrier can be generated using the fundamental output of the synthesizer, as the maximum frequency to be synthesized – 108 MHz – is 45% of the sampling frequency. This way, the use of one of the typical aliased images by lower speed DDS devices as the RF transmitted signal no longer becomes necessary, improving the output signal-to-noise ratio and reducing the output filter complexity. This can be a simple low-pass filter can be used instead of a harder to design band-pass one. The design of the RF low-pass filter will be explained in the next section.

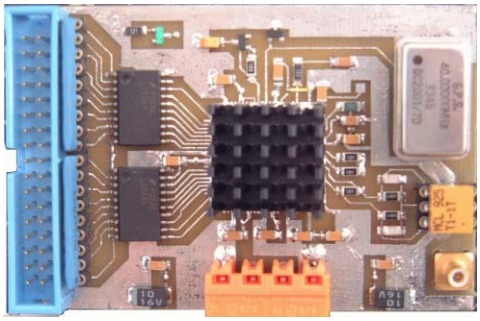


Figure 4: Direct digital synthesizer board

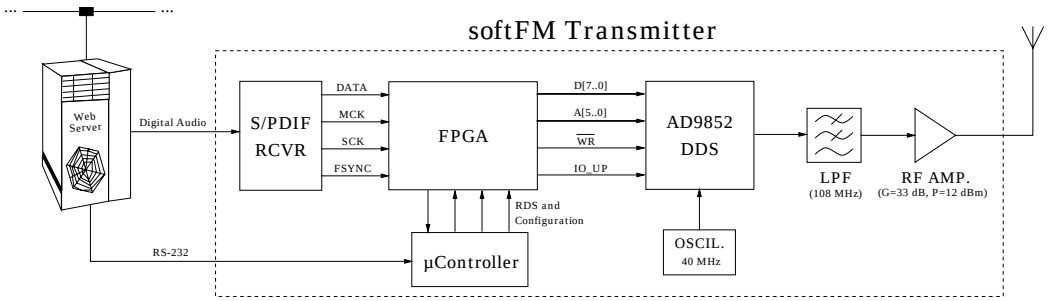


Figure 2: softFM block diagram.

3.4 Low-pass filter and RF amplifier

The main purpose of the low-pass filter is to attenuate all the unwanted spectral images and harmonics typically present at the output of a DDS system [6]. Those spectral images appear around multiple integers of the sampling frequency (f_{clk}), at $kf_{\text{clk}} \pm f_{\text{out}}$, $|k| \geqslant 1$, where f_{out} is the fundamental output frequency. In this system's case, the worst situation is when the carrier frequency is set to 108 MHz and the first alias is located at $240 - 108 = 132$ MHz. To considerably attenuate this alias, a very steep roll-off filter is needed. The Cauer-Chebyshev (CC) or elliptic filter is the type of filter that provides steepest transition from passband to stopband for a given filter order. A seventh-order Cauer-Chebyshev low-pass filter was designed and its frequency response characteristic is shown in Figure 5. Lower order filters could not provide an adequate stopband rejection for the required filter roll-off.

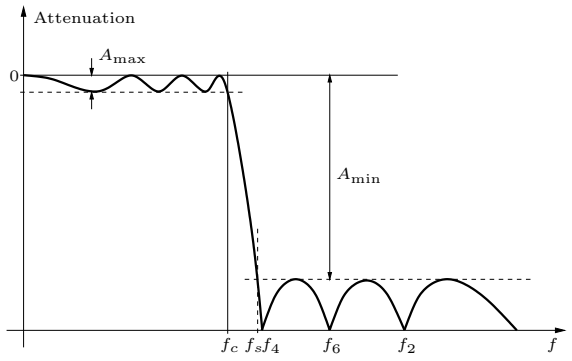


Figure 5: Frequency response of a seventh-order Cauer-Chebyshev filter

As can be noticed, the response has tree frequency notches in the stopband region: f_4, f_6 e f_2. In order to attain maximum rejection of the worst case alias, one can specify the f_4 parameter to be located in the region of that alias. The following procedure should be followed for maximum alias attenuation:

- $f_4 = f_{\text{clk}} - \text{mean}(f_{\text{out}})$ if $f_{\text{clk}} - \max(f_{\text{out}}) > f_s$, otherwise,
- $f_s = f_{\text{clk}} - \max(f_{\text{out}})$

Initially, the synthesizer clock frequency was set to $f_{\text{clk}} = 280$ MHz and the present filter was optimized for that value (this frequency reduction had to be done due to the overheating of the DDS device) . The design procedure follows:

1. The first step was to choose f_c and $A_{\max}$ (passband ripple). In this case $f_c = 108$ MHz and $A_{\max}$ =0,01 dB which is equivalent to a maximum reflection coefficient $\rho = 5\%$. These two are related by [7]: $A_{\min} = -10\log_{10}(1 - \rho^2)$.
2. After a table look-up in a catalog of normalized CC filters [7], for $f_4 = f_{\text{clk}} - \text{mean}(f_{\text{out}}) = 280 - 98 = 182$ MHz, f_s will be 179 MHz.
3. The previous value for f_s do not verify the condition $f_{\text{clk}} - \max(f_{\text{out}}) = 280 - 108 = 172 > f_s$. In this case, f_s had to be set to $f_{\text{clk}} - \max(f_{\text{out}}) = 172$ MHz. The new vale of f_4 is 175 MHz
4. The remaining parameters, obtainde from the filter table, are: $A_{\min} = 67$ dB (stopband rejection), $f_6 = 210$ MHz and $f_2 = 359$ MHz.

The design parameters for this filter are grouped in table 1.

Table 1: Cauer-Chebyshev filter parameters

Parameter	Symbol	Value
Order	n	7
Cutt-off frequency	f_c	108 MHz
Stopband frequency	f_s	172 MHz
Passband ripple	$A_{\max}$	0,01 dB
Stopband rejection	$A_{\min}$	67 dB
Input/output impedance	Z_0	50 Ω

The structure of this filter is depicted in Figure 6 and the resultant nearest standard capacitor and inductor values presented in Table 2.

Table 2: Component values of the designed filter

Component	C1	C2	C3	C4	C5	C6	C7
Value (pF)	22	1.8	47	8.2	39	6.8	18
Component	L2	L4	L6				
Value (nH)	100	100	82				

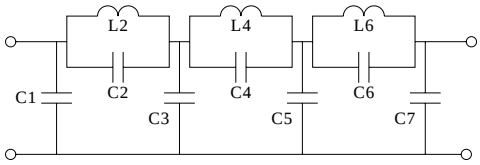


Figure 6: Seventh-order Cauer-Chebyshev filter structure

The filter transfer function is plotted in Figure 7 and compared to the Spice3 simulation results (dashed line). There is a slight difference in the actual f_s, f_4 and f_6 frequencies and a considerable deviation in the $A_{\min}$ parameter (yet an attenuation higher than 50 dB up to 300 MHz is achieved). These deviations are due to tolerances and quality of the components (lower loss capacitors and higher Q inductors should have been used).

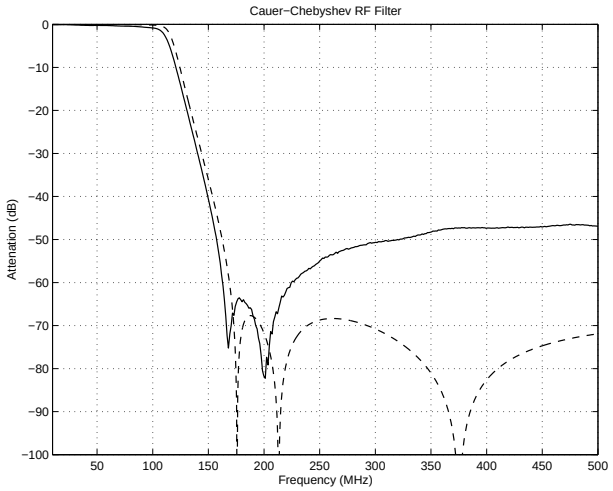


Figure 7: Actual and simulated filter frequency responses

The output signal is further amplified using an RF amplifier based on the Minicircuits MAR-8SMs model [8]. This amplifier provides a gain of 33 ± 0.05 dB in the FM band (87.5–108.0 MHz) and an output power of 11 dBm. This power level will be sufficient to drive a medium power amplifier (like 1W) to extend the transmitter range.

Images of both amplifier and filter can be found in Figure 8. The components used were all surface mount devices (SMD) aiming at performance optimization.

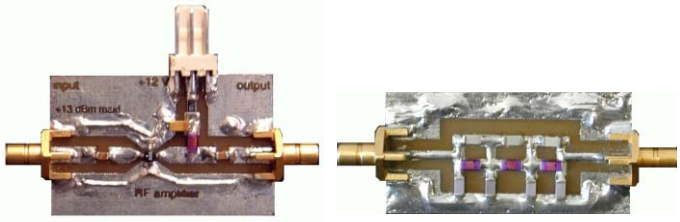


Figure 8: PCB images of the designed filter and amplifier (left image)

3.5 System management and configuration

The softFM transmitter can be controlled via a GUI (Graphical User Interface) accessible via the HTTP protocol. This GUI was built in HTML and JavaScript programming languages, and runs on a standard PC. The communication with the transmitter is done using an RS-232 link.

There are two modes of operation: *user mode* and *administration mode*:

- the *user mode* is accessible by all users where the preferred musical themes can be chosen from a data base and added to a play list. Requests are processed on a first-come-first-serve basis. The audio files are output via a sound card equipped with an S/PDIF interface.
- the *administration mode* requires user authentication. This mode is intended to perform system configuration. The following RDS parameters can be programmed: PI (Program Identification code), PS (Program Service name), TA (Traffic Announcement), TP (Traffic Program), PTY (Program Type code) and RT (Radio Text). The RF carrier frequency as well as the maximum frequency deviation can also be programmed within this mode.

The communication between the Web server and transmitter server follows the UECP (Universal Encoder Communication Protocol) standard [9] that specifies a common data interface and protocol for controlling RDS encoders.

4 Experimental results

From the transmitter tests performed so far, an excellent audio quality in terms of distortion and stereo separation were observed.

Several spectrum plots obtained are presented next.

In the first one (Figure 9) a 100 MHz carrier along with the aliased images and harmonics can be observed. The worst case alias, located at 140 MHz, is approximately 39 dB down the carrier level. This alias could be considerably reduced if the CC filter had been specified having a clock frequency of 240 MHz in mind and not the initial one of 280 MHz.

The following plots (Figure 10) show the detail of the carrier for a maximum frequency deviation of $\Delta f = 75$ kHz under two conditions:

- when no audio signal exists (only the 19 kHz pilot tone is present at a 10% level) the spectrum is discrete in nature as theoretically expected, with spectrum components 19 kHz apart and amplitudes given by the Bessel functions.
- when the modulating signal is a 1 kHz sine wave at fullscale, the occupied bandwidth is approximately 150 kHz as predicted by Carson's rule ($\mathrm{BW} \approx 2\Delta f + 2f_{\max}$) [10].

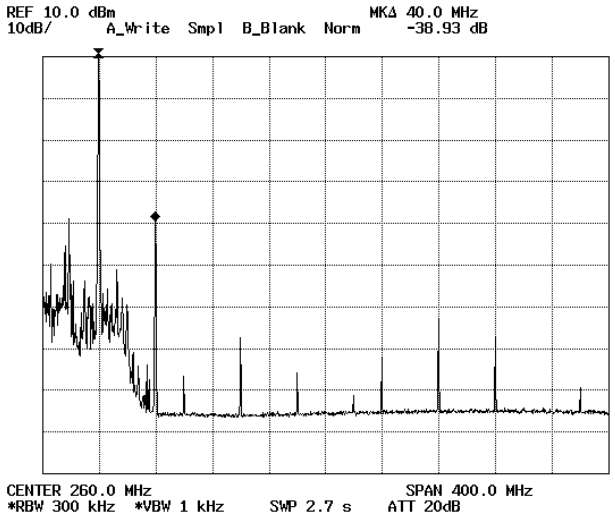
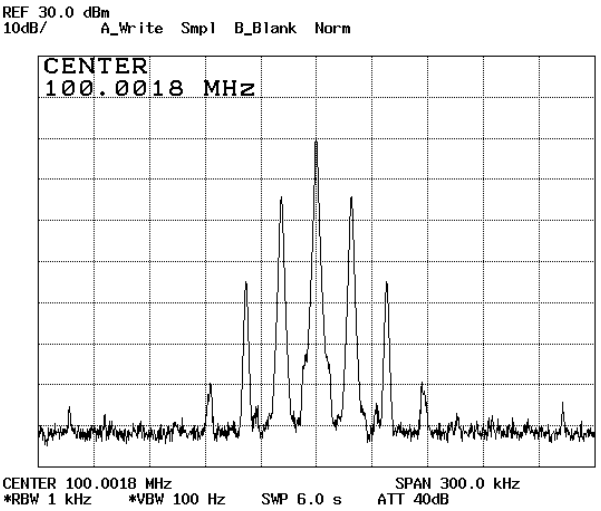
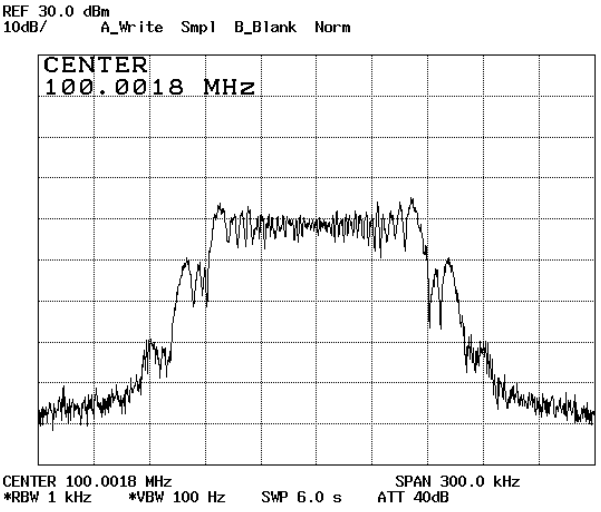


Figure 9: Overall spectrum plot for a carrier frequency of 100 MHz



(a) unmodulated carrier (19 kHz pilot tone only)



(b) modulated with a 1kHz sine wave at 0 dBFS

Figure 10: Detail of the carrier spectrum

5 Applications and further work

As the baseband signal processing is software defined, the system can be easily upgraded to support upcoming features like DARC (Data Radio Channel), which is a technology that allows the transmission of data at 16 kbit/s on a 76 kHz subcarrier of the MPX spectrum.

The softFM system can be used in a scenario where a completely automated and remotely operated radio station must be deployed. This system can also be used to build up broadcast stations whose program line-up is under control of the listeners.

Further developments in this system include the redesign of the low-pass CC filter to better reject the unwanted spectrum aliases and spurious responses of the synthesizer; upgrade the signal processing subsystem with a higher density FPGA to enhance the computation precision and to accommodate other features like DARC; and finally the construction of a medium power RF amplifier that would extend the maximum range which is very reduced at this time (less than 1 km).

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