**Monday, June 18th**

**9:00 - 9:10 Welcome Address**

**9:10 - 10:00 Invited Talk – Testing Low Power Digital IC’s May Require Mixed-Signal Test Solutions**
Joan Figueras, Universitat Politècnica de Catalunya

10:00-10:20 **Poster Session 1**

**10:20-10:50 Break, Poster Session 1**

**10:50-12:30 Session 1 – Analogue Testing**
Moderator: Jacob Abraham and Hans Kerkoff

**12:30-14:00 Lunch**

**14:00-15:15 Session 2 – Mixed-Signal Test**
Moderator: Salvador Mir and Bernd Straube

**15:15 -15:45 Break**

**15:45-17:25 Session 3 – RF Testing**
Moderator: Abhijit Chatterjee and Francisco Beltrán

**18:00 – Welcome reception**
10:20-10:50 Break
10:50-12:30 Session 5 – GHz/Gbps testing
Moderator: Andre Ivanov and Ana Leão
S5.1 Testing SerDes ICs beyond 4 Gbps – new priorities
Stephen Sunter, Aubin Roy, LogicVision (Canada); Abhijit Chatterjee, Georgia Tech (USA)
S5.2 A Novel Built-in Test Technique for Phase/Frequency Modulated RF Transmitters
Hyon Choi, Donghoon Han, Abhijit Chatterjee, Georgia Institute of Technology, Atlanta, USA
S5.3 Design and Implementation of Low Noise and High Speed Multi-layer Test Board with High Performance 3D-EBG Structure
Kijae Song, Samsung Electronics, Korea
S5.4 MEMS Switches and SiGe Logic for Multi-GHz Loopback Testing
David C Keezer, Dany Minier, Patrice Ducharme, Doris Viens, Greg Flynn, John Mckillop, Georgia Institute of Technology, Atlanta, USA, IBM, Bromont, Canada, TeraVista, Austin, USA

12:30-14:00 Lunch
14:00-15:45 Panel Discussion - Test limits in a microvolt, nanometer, picosecond world
Organizers: Stephen Sunter, LogicVision (Canada); Abhijit Chatterjee, Georgia Tech (USA)
Moderator: Stephen Sunter
Panelists: Jacob Abraham, University of Texas (USA); Bozena Kaminska, Pultronics (Canada); David Keezer, Georgia Tech. (USA); Anne Meixner, Intel (USA); Andrew Richardson, University of Lancaster (UK)

Abstract: Are we approaching the practical or meaningful limits to production testable performance? Traditionally, test capability is required to be an order of magnitude better than the performance being tested. As thermal noise, EMI, wire bandwidth, and process variability increasingly impair testability, can we test adequately and economically? An IC’s performance beyond 5 GHz, 5 Gbps, 16-bit quantization, or 90 nm can vary greatly in a system compared to its ATE-verified performance. Will IC performance become too dependent on the system? What is the right balance between test simplicity and fault coverage for these circuits? Is picosecond or microvolt accuracy necessary for testing? Are designs good enough that such detailed parametric testing can be avoided, or do manufacturers ignore performance variability because it depends on many aspects of a system (and test equipment) and errors can’t be traced to one device? If a picosecond or microvolt matters, then perhaps testing is not the place to detect it, and the system should be designed to tolerate this inaccuracy inherently.

16:00 - Social event

Wednesday, June 20th

9:00 - 9:40 Invited Talk - The Challenges of MEMS Testing
Shawn Blanton, Carnegie Mellon University

9:40-10:20 Poster Session 2
Moderator: Florence Azäis
P2.1 A Novel Binary Search Method for Characterizing Hysteresis Featured in Integrated Circuits
Weishu Wu, Texas Instruments
P2.2 Mixed-signal Design of Dynamic Delay Buffers to Improve Tolerance to Power Supply and Temperature Variations
Jorge Semião, João Paulo Teixeira, Isabel Teixeira, Fabian Vargas, Juan J. Rodríguez-Andina, Judit Freijedo, Escola Superior de Tecnologia - Universidade do Algarve, IST/INESC-ID, Portugal, Catholic University - PUCRS, Brazil, University of Vigo, Spain
P2.3 Considerations for FPGA Integration into the ATE Device Interface Board
Ian Groul, Thomas Oshea, Jeffrey Ryan, University of Limerick, Ireland
P2.4 Layout-Oriented Fault Analysis for DRAM Design Components
Martin Versen, Jelena Knežević, Sergio Montoya, Torsten Coym, Wolfgang Vermeiren, Bernd Straube, Qimonda AG, Fraunhofer Inst. für Int. Schaltungen (IIS), Germany
P2.5 Accurate Linearity Testing of A/D Converters in the Presence of Ground Bounce Noise
Shalabh Goyal, Abhijit Chatterjee, Georgia Institute of Technology, USA
P2.6 White Noise Signal Generator for ADC Testing
Josef Vedral, Jan Neškudla, CTU FEE Prague, Czech Republic

10:20-10:50 Break, Poster Session 2
10:50-12:30 Session 6 – MEMS Testing
Moderator: Bernard Courtouquis and Marcin Marzencki
S6.1 Layout-Based Fault List Generation and Fault Simulation for DNA Sensor Arrays Testing
Daniela de Venuto, Danilo Laterza, Politecnico di Bari, Italy
S6.2 Self-Testing of Micro-Electrode Array Implemented as a Bio-Sensor
Josef Vedral, Jan Neškudla, CTU FEE Prague, Czech Republic
S6.3 Capacitive MEMS accelerometers testing mechanism for auto-calibration and long-term diagnostics
Delft University of Technology, The Netherlands, University of British Columbia, Canada, INESC Porto, Portugal
S6.4 A Fault-Tolerant MEF Peptide Synthesizer using Sense-Electrode
Xiao Zhang, Hans Kerkhoff, Frédéric Mailly, Pascal Nouet, Hongyuan Liu, Andrew Richardson, TDT, CTIT, University of Twente, The Netherlands, LIRMM, France, Lancaster University, United Kingdom

12:30-14:00 Lunch
14:00-16:05 Session 7 – ADC Test
Moderator: Jose Huertas and Andrew Richardson
S7.1 A Simple Method for Linearity Testing of ADCs Using Nonlinear Test Stimuli
Esa Korhonen, Juha Kostamovaara, University of Oulu, Electronics Laboratory, Finland

S7.2 Postprocessing Measurement Data---Are You Using the Correct Algorithm?
Carsten Wegener, Infineon Technologies AG, Germany

S7.3 Fully-Efficient ADC Test Technique for ATE with Low Resolution Arbitrary Wave Generators
Vincent Kerzééro, Philippe Cauvet, Serge Bernard, Florence Azalís, Michel Renovell, Mariane Comte, NXP, LIRMM, LIRMM, France

S7.4 Simple evaluation of the non-linearity signature of an ADC using a spectral approach
Eduardo Peralias, M. Angeles Jalon, Adoracion Rueda, IMSE-CNM, Universidad de Sevilla, Spain

S7.5 A Methodology for Structural Test of Folded ADCs
Roman Mozuelos, Yolanda Lechuga, Mar Martinez, Salvador Bracho, University of Cantabria, Spain

16:05-16:20 Closing Session