Abstract: The testability structure for digital circuits described in IEEE Std 1149.1 has been extended to provide similar facilities for mixed-signal circuits. The architecture is described, together with the means of control of and of access to both analog and digital test data. Sample implementation and application details (which are not part of the standard) are included for illustrative purposes.

Keywords: analog test, mixed-signal test, boundary-scan, design for testability, board testing, in-circuit test.
Introduction

(This Introduction is not a part of P1149.4 - Mixed-Signal Test Bus)

The development of this standard began with a preliminary meeting in the summer of 1991, when the need was recognized for a standardized structure to be incorporated into mixed-signal circuits to combat the testability problems posed by such circuits. This meeting adopted as its mission

To define, document, and promote the use of a standard mixed-signal test bus that can be used at the device and assembly levels to improve the controllability and observability of mixed-signal designs and to support mixed-signal built-in test structures in order to reduce both test development time and testing costs, and to improve test quality.

The work received the support of the Test Technology Technical Committee of the Computer Society in November 1991, and the Working Group started work under the Chairmanship of Prof. Mani Soma. In January 1995, Professor Soma resigned as chair and Adam Cron was elected chair of the Working Group.

At the time of issue of this draft, the members of the Working Group were:

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In the development of this Standard, the Working Group was supported by many other individuals from many different organizations who contributed time, administrative effort, and technical suggestions.
In particular, the working group wishes to acknowledge the contributions made by the following individuals:

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Standard for a Mixed-Signal Test Bus

1 Overview

1.1 Organization of the standard

This standard is divided into ten clauses.

Clause 1 describes the scope and objectives of the standard, and explains how the material of the standard is organized.

Clause 2 lists references to related standards necessary for the understanding of this standard, while Clause 3 defines terms and acronyms.

Clauses 4 to 8 contain specifications for the particular features of this standard, together with descriptive material that illustrates the need for the specified features or their application. This descriptive material is intended to place the details of various parts of the design in perspective and to provide examples of implementation and use.

Clause 9 addresses some of the practical issues that will arise in the implementation of the standard; in particular, it defines the performance required from a compliant part, and describes how the performance limits can be measured.

Clause 10 summarizes the conditions under which any particular component can claim conformance to the standard, and defines the documentation that must be provided by the manufacturer to allow test equipment to make use of the test features.

1.2 Context

Figure 1 illustrates the context within which this standard is intended to operate. It shows an electrical circuit constructed as a printed circuit assembly (PCA) consisting of a substrate carrying a pattern of conductors (the interconnect) on which separately manufactured components are mounted so that the component pins make electrical contact with the interconnect. In normal functional operation, the PCA connects to other parts of the system by way of a set of contacts such
as the edge-connector shown in Figure 1.

Figure 1: Mixed-signal printed circuit assembly

In Figure 1, the component that is the subject of this standard is shown shaded. In a typical mixed-signal PCA, the pins of the component may be connected to

- other mixed-signal components (labelled M), which may or may not conform to this standard;

- digital components (labelled D), which may or may not conform to IEEE Std 1149.1;

- analog components (labelled A), which could be anything from a single transistor to an operational amplifier or an analog signal processing circuit, but which would be unlikely to contain any associated testability features;

- discrete components (labelled C), such as pull-up resistors or coupling capacitors, which will not have any associated testability features.

The PCA is tested, both in production (to verify correct manufacture) and in field service (to detect and locate faults), using automatic test equipment (ATE) to supply test signals to, and to collect test responses from, some or all of the component pins. The aim of the test structures described in this standard is to provide test access to individual component pins from the edge-connector, so as to reduce or eliminate the need for the ATE to make direct physical contact via mechanical probes. The extent to which this aim can be satisfied will depend on the make-up of the PCA: the pins of those
components that conform either to this standard or to IEEE Std 1149.1 will be accessible from the edge-connector, and this will provide at least partial access to the pins of some non-conformant components. If this is inadequate for testing purposes, additional probe access would need to be employed.

1.3 Scope of the standard

1.3.1 Aims

This standard defines test features to be included in a mixed-signal (analog and digital) component, together with associated test protocols, to provide standardized approaches to:

- Interconnect Test: Testing for opens and shorts among the interconnections in a PCA;
- Parametric Test: Making analog characterization measurements, and testing for presence and value of discrete components in a PCA;
- Internal Test: Testing the internal circuitry of the mixed-signal component itself whether or not it is part of a PCA.

The standard does not mandate implementation details of the test circuitry, although examples of conformant implementations are given for illustrative purposes.

1.3.2 Interconnect testing

IEEE Std 1149.1 provides an effective mechanism for interconnect testing of a PCA populated with digital components. The first objective of this new standard is to provide a similar capability for an assembly such as that illustrated in Figure 1, populated with analog, digital, and mixed-signal components, together with discrete components.

In seeking to satisfy this objective, one of the fundamental requirements is to provide the ability to detect open circuits in the interconnections between integrated circuits, and to detect and diagnose bridging faults anywhere in the interconnect regardless of whether they normally carry digital or analog signals. The aim also is to provide a structure that allows testing in full compatibility with IEEE Std 1149.1, so as to permit mixed-signal interconnect testing to take place at the same time, and using the same procedures, as digital interconnect testing.
The range of problems is illustrated in Figure 2, which shows a group of interconnected components mounted on a board or other substrate, analog and digital pins being represented by “A” and “D” respectively. The left hand side of Figure 2 shows open circuits in analog and digital lines and also in an analog interconnection network. The right hand side of Figure 2 shows a number of short circuits: it should particularly be noticed that short circuits can occur between analog and analog, digital and digital, and analog and digital lines, as well as across discrete components in interconnection networks.

1.3.3 Parametric Test

The second objective of this standard, parametric test, recognizes the fact that groups of one or more discrete components are often interposed between integrated circuits, performing functions such as level shifting, passive filtering, and ac coupling. The inclusion of discrete components in the interconnection pathway gives rise to the concept of “extended” (as opposed to “simple”) interconnect, as illustrated in Figure 3: to provide for the testing of components in an extended interconnect, the standard defines a framework that will support analog measurements, allowing, for example, impedances of discrete components to be computed. Meeting this objective also allows testing of components such as pull-ups and filter capacitors associated with either analog or digital components.

Also illustrated in Figure 3 is an example of differential interconnect, which is a pair of pathways carrying signals whose information content is defined by the pair of signals rather than by either one signal individually. In the case of digital differential interconnect, these pathways would normally be excited by a single signal, and the activity would be converted back to a single signal after reception. Analog differential interconnect could follow the same pattern, but conversion from or to a single-
ended form might take place within the core, or it might not take place at all. Differential interconnect can be treated either as two separate simple interconnects, testing the structural connection between pins, or as a single extended interconnect, testing the functional connection between single-ended transmission point and single-ended reception point.

A similar situation from the testing point of view is illustrated in Figure 4, where an analog signal to be transmitted is first passed through an analog-to-digital converter, transmitted as a parallel set of digital signals, and passed through a digital-to-analog converter to form a received analog signal. Again, the interconnect can be tested as several separate simple digital interconnects, and then by treating it as if it were a single analog connection between the transmitted and received signals, thereby allowing the overall transmission properties of the system to be assessed.
1.3.4 Internal test

The third objective of this standard, internal test, relates to the ability to perform comprehensive tests on the components either in isolation or while mounted on a substrate. Since this may require the incorporation of internal test structures whose impact on the cost and performance of the circuit may be deemed unacceptable, this aspect of the standard is not mandatory. The addition of designer-defined test functions is not limited by this standard, which allows for the incorporation of ad hoc testability features within the internal core structure. To make such features accessible to the end-user, it is important that they are fully documented (see 10.2).

1.4 Background reading

Those unfamiliar with IEEE Std 1149.1 might find it helpful to study some of the following books and papers, some of which also discuss mixed-signal testing using structures related to this standard.


A test programmer’s perspective of IEEE Std 1149.1, describing the introduction of the system into a manufacturing company.


A description of a node-voltage based fault detection and diagnosis process for systems utilizing 1149.4 technology.


A description of the main features of IEEE Std 1149.1, together with examples of implementations and use. Contains an extensive bibliography, and reproduces 16 key papers (mostly from ITC Proceedings and other IEEE publications).

A description of the design and use of IEEE Std 1149.1 and of this standard, written from the point of view of practicing test engineers.


A detailed description of a metrology whereby the values of components connected between integrated circuits may be calculated, using a test structure similar to the one described in this standard.
2 References

This standard shall be used in conjunction with the following publications.


NOTE - All IEEE standards are revised periodically. The next revision of IEEE Std 1149.1 will contain updated versions of all the material at present contained in IEEE Std 1149.1a and IEEE Std 1149.1b, and is expected to be fully consistent with the present standard.

3 Definitions, acronyms, and voltage symbols

3.1 Definitions

The following terms are used within this standard.

3.1.1 analog boundary module (ABM): a circuit module connected between the core circuit and an analog function pin to provide facilities for test in a mixed-signal integrated circuit. See: core circuit, function pin, mixed-signal circuit.

NOTE - An ABM may be attached to a digital function pin in order to provide analog measurement capability to the pin.

3.1.2 analog pin: a pin on an integrated circuit or other component that is intended to pass information represented as a current or voltage that can have any value between the limits defined by the driver or receiver to which it is connected. Contrast with: digital pin.

NOTE 1 - Analog pins can have several forms. In addition to input, output, and bidirectional pins which are analogous to corresponding digital forms, it is possible to have pins that do not readily fit into any of these categories (e.g., those supporting compensation elements for operational amplifiers). Any such pin that has no identifiable drive capability should be regarded for the purposes of this standard as an input pin.

NOTE 2 - An analog pin may be put into a state in which no signals can pass in either direction between the pin and the core circuit. See: high-Z, core circuit, core disconnect.

NOTE 3 - An analog pin can pass digital data, using discrete levels that lie within its analog range.

3.1.3 analog test access port (ATAP): a set of two mandatory and two optional pins on a mixed-signal integrated circuit. The pins are connected to a bus allowing automatic test equipment to gain access to on-chip analog test facilities. The mandatory pins are labelled AT1 and AT2; the optional pins (labelled AT1N and AT2N) are normally used for differential testing.

3.1.4 CD State: the state of an analog pin when it is isolated from the core circuit and all test circuits. See also: core disconnect, residual element.

NOTE - When a pin is in the CD state, there may be residual elements to which it remains connected.

3.1.5 compliance-enable pins: a set of one or more pins on a component such that full compliance with the rules of this standard is assured only when a defined pattern of enable
signals (a compliance-enable pattern) is applied to the compliance-enable pins.

NOTE - There may be more than one compliance enable pattern.

3.1.6 conceptual switch: a circuit feature, acting under the control of a digital control signal, that allows two circuit nodes to be electrically connected or isolated, as though there were a switch between them. See: switch.

NOTE 1 - Depending on physical constraints, such as size, power consumption, and electrical characteristics, it may be possible in any particular application to implement all, some, or none of the conceptual switches by conventional CMOS transmission gates.

NOTE 2 - The symbols shown in Figure 5 are used to represent conceptual switches in this standard. For a switch with active high control (Figure 5(a)), the switch is closed (Data line 1 = Data line 2) when Control = logic 1; for a switch with active low control (Figure 5(b)), the switch is closed when Control = logic 0. See logic 0, logic 1.

3.1.7 core circuit: that part of the circuitry in an integrated circuit that provides the intended data manipulation function (as distinct from dedicated test circuitry). See also: residual element.

NOTE 1 - The core circuit is analogous to the “system logic” in IEEE Std 1149.1.

NOTE 2 - Residual elements, which are permanently connected to the pin (i.e., in test mode as well as in normal function mode), are not regarded as being part of the core circuit.

3.1.8 core disconnect: a facility provided within an analog boundary module (usually mediated by a conceptual switch) which allows a pin to be disconnected from the core circuit, such that the signal at the pin can be driven to any value within the pin's normal functional range without affecting the core circuit, and such that no value generated in the core circuit will affect the pin. See: conceptual switch, core circuit. See also: high-Z, residual element, CD state.
NOTE 1 - The core disconnect facility could be provided as part of the functional driver or receiver attached to the pin, e.g., by implementing a driver with high-Z capability.

NOTE 2 - It is necessary to document all residual elements that remain connected to the pin when it enters the CD state.

3.1.9 differential interconnect: a pair of connections carrying signals from a transmitter on one component to a receiver on another component, where the transmitted information (which may be either analog or digital) is represented by the difference between two signals rather than by either signal individually. See also: simple interconnect; extended interconnect.

3.1.10 digital boundary module (DBM): a circuit module connected between the digital core circuit and a digital function pin to provide facilities for test in a digital or mixed-signal component. A DBM serves the same function as, and conforms to the same rules as, the boundary-scan register cells defined in IEEE Std 1149.1.

NOTE 1 - A DBM may contain one or more boundary-scan register cells as explained in IEEE Std 1149.1.

NOTE 2 - A DBM may also be interposed at the boundary between the digital and analog portions of the core circuit.

NOTE 3 - A control-and-observe DBM includes a switching function in the serial data path between pin and core; an observe-only DBM captures data from the data path without interrupting it.

3.1.11 digital pin: a pin on an integrated circuit or other component that is intended to pass data represented as a voltage or current that can have one of two discrete values. Contrast with: analog pin.

NOTE 1 - In this standard the two discrete values are referred to as logic 0 and logic 1. See: logic 0, logic 1.

NOTE 2 - In addition to the set of discrete data values, a digital pin may be put into a state in which its driver is disabled, so that it cannot actively sink or source current, and therefore cannot influence the state of the attached net. See: high-Z, net.

NOTE 3 - If analog data is applied externally to a digital input pin, the internal circuitry will normally interpret the data as digital. Use of the pin in this way will need to have due regard to possible adverse effects on the internal circuitry (e.g., power consumption).

NOTE 4 - A digital function pin may have additional circuitry to allow analog signals to be applied or monitored for test purposes. This would not affect its status as a digital pin.

3.1.12 discrete component: an electrical element that is mounted on a printed circuit board or other substrate and connected to the interconnect wiring system, but which is not integrated to any significant extent with other elements, and does not contain boundary module test
circuitry adjacent to its pins. *See: interconnect.*

3.1.13 **extended interconnect**: a connection pathway consisting of two or more nets that includes one or more discrete components. *See: net. Contrast with: simple interconnect. See also: discrete component.*

NOTE - The test requirement is to verify both the integrity of the connections and the values of the components.

3.1.14 **function pin**: an analog or digital pin on an integrated component that takes data into and/or out of the core circuit when operating in normal function mode. *Syn: mission pin, system pin.*

NOTE: All pins carrying signals that affect the behaviour of the component, including reference supply pins but excluding power supply pins and compliance-enable pins, are regarded as function pins.

3.1.15 **high-Z**: a condition in which the driver on a pin is inactive. The state of a net attached to a pin that is at high-Z is determined by values applied to other parts of the net. *See: net. Contrast with: CD state. See also: core disconnect.*

NOTE: For the purpose of this standard, the impedance looking into a pin that is at high-Z must be > 1MΩ for any signal between V_DD and V_SS at any frequency up to 10 kHz.

3.1.16 **in-circuit testing**: A method of testing a printed circuit assembly by making direct physical contact between automatic test equipment and nets that are connected to the pins of individual components. *See: net.*

3.1.17 **interconnect**: the system of wiring that carries data and control signals between the different components mounted on a printed circuit assembly. *See also: simple interconnect; extended interconnect; differential interconnect.*

3.1.18 **internal test bus**: the system of wiring that carries analog test signals around the interior of an integrated circuit. *See: test bus interface circuit.*

3.1.19 **logic 0, logic 1**: The two logic voltage levels for digital signals. In positive logic systems, the more positive of the two logic voltage levels is taken to be logic 1.

NOTE 1 - For convenience, positive logic is assumed throughout this standard.

NOTE 2 - The voltage levels representing logic 0 and logic 1 are not necessarily the same at every function pin.

NOTE 3 - logic 0 and 1 are often represented as LO and HI respectively.
3.1.20 **mixed-signal circuit**: a circuit in which some variables are represented by analog (continuously variable) quantities, and some variables are represented by digital (discrete) quantities.

3.1.21 **net**: an interconnection path between component pins, where the resistance of the path is not significantly different from zero.

3.1.22 **reference quality voltage**: dc source capable of sourcing and sinking current over a defined range without appreciable change of voltage, and whose stability over a given time interval is guaranteed.

NOTE - Whether or not a given voltage source is of reference quality has a major impact on the accuracy of the measurement capabilities of the structures described in this standard.

3.1.23 **residual element**: a circuit element that is part of a network connected to one or more function pins, and that, for operational reasons, cannot be isolated from the pins in test mode. The network of residual elements can be connected to power supply pins as well as to function pins, provided it can be modelled, over a defined working range, by a network of ideal resistors, capacitors, and inductors together with independent dc sources.

3.1.24 **simple interconnect**: a connection between two or more component pins consisting only of a net. *Contrast with: extended interconnect.*

3.1.25 **switch**: in the context of this standard, a switch is an electronic device connected between two data lines. It can exist in one of two states, referred to as "open" and "closed", the state at any time depending on a digital control variable. When the switch is open, the pathway between the two data lines has a very high impedance (ideally infinite), so that signals appearing on the data lines should be completely independent. When the switch is closed, the pathway between the two data lines has a very low impedance (ideally zero), so that signals on the two data lines should be identical.

NOTE 1 - Practical electronic switches implemented in silicon depart from the ideal in at least three ways.

(a) In the "on" state, the pathway between the two data lines may have significant impedance, or the relationship between voltage and current may be non-linear (e.g., a voltage-dependant “impedance”).

(b) In the "off" state, there may be significant interaction between the signals on the two data lines due to (e.g.) stray capacitance.

(c) In either state there may be significant leakage pathways through which current can pass from the data
The effects of all these characteristics will need to be considered as part of the detailed implementation, especially in a system containing multiple-switch networks.

NOTE 2 - A switching action effectively in series with the function signal pathway can sometimes be obtained without a physically separate device by incorporating a high-Z or enable facility into the functional circuitry. See: conceptual switch, high-Z.

NOTE 3 - Data transmission through a switch is normally assumed to be bi-directional (as with electromechanical devices such as relays or semiconductor switches such as transmission gates). Some forms of switch can implement only uni-directional voltage or current dependence.

3.1.26 test access port (TAP) : The test access port defined by IEEE Std 1149.1. Contrast with : ATAP.

3.1.27 test bus interface circuit (TBIC) : a circuit module that allows an internal analog test bus in an integrated circuit to be isolated from or connected to the pins in the ATAP. See : ATAP.

3.1.28 test data : data that is entered into an electronic system of any kind (component, printed circuit assembly, sub-system, system) for the purpose of verifying the integrity of part or all of the system. Test data may be entered through function pins or test pins or both.

3.1.29 test pin : a pin on a component or a printed circuit assembly that is provided solely or primarily for use during test or maintenance operations.

3.2 Acronyms

ABM : Analog Boundary Module

ATAP : Analog Test Access Port

ATE : Automatic Test Equipment

CUT : Circuit Under Test

DBM : Digital Boundary Module

PCA : Printed Circuit Assembly
TBIC : Test Bus Interface Circuit
TAP : Test Access Port

3.3 Voltage source symbols

Several voltage sources are required as part of the internal test structure described in this standard. The symbols used to denote these voltage sources are defined below. All of these sources are, in general, pin-specific,

\( V_{\text{clamp}} \): a fixed voltage that can be applied to internal test buses when not in use to reduce the possibility of noise, crosstalk, or feedback.

\( V_{G} \): a pin-specific reference quality voltage that is supplied to a component at a pin. Any function pin can be connected to \( V_{G} \) through its analog boundary module. See: reference quality voltage.

NOTE - \( V_{G} \) would normally be one of the power supply rail voltages.

\( V_{H}, V_{L} \): two dc voltages used as test signals on analog pins during interconnect testing and component measurement.

NOTE 1 - \( V_{H} \) and \( V_{L} \) are pin-specific, and typically \( V_{H} > V_{L} \).

NOTE 2 - At output pins, \( V_{H} \) and \( V_{L} \) will be supplied from the functional driver, and will correspond to logic 1 and logic 0 respectively.

\( V_{TH} \): A pin-specific voltage to which the voltage at a function pin is compared. The result of the comparison is a binary value that can be captured in the boundary-scan register.

The meaning of other terms used in this standard shall be as defined in IEEE Std 100-1996.
4    Testability Architecture

4.1  Overview

4.1.1  Specification

Rules

(a)  The component shall conform to all provisions of IEEE Std 1149.1 except where specifically noted herein.

NOTE 1 - This rule implies that a component conforming to this standard must contain a TAP to provide access to the circuit for digital test signals. This TAP will contain three input lines (TDI, TCK, TMS), and one output line (TDO); it may contain an optional fourth input line (TRST*).

NOTE 2 - In accordance with the rules of IEEE Std 1149.1, a component may require the application of a particular pattern of signals (a compliance-enable pattern) to a set of one or more compliance-enable pins before the component is brought into full compliance with this standard. There may be more than one compliance-enable pattern for a particular component.

NOTE 3 - The version of IEEE Std 1149.1 referenced in Clause 2 makes little provision for testing the analog portions of a mixed-signal chip, and contains a few rules relating to analog pins that are not compatible with the provisions of this standard. These inconsistencies are indicated in this standard, and may be resolved in a future revision of IEEE Std 1149.1.

(b)  The interpretation of the rules governing those structures and facilities that are common to this standard and to IEEE Std 1149.1 shall be determined by IEEE Std 1149.1.

NOTE - This rule implies that, when implementing this standard, the structure and performance of those elements described in IEEE Std 1149.1 must be in accordance with the specifications set out in IEEE Std 1149.1.

4.1.2  Description

This standard is an extension of IEEE Std 1149.1, and consists of additional structures to be added to an IEEE Std 1149.1-conformant chip. Components that are conformant with this standard, when mounted on a common substrate together with IEEE Std 1149.1-conformant chips, allow common test operations (in particular, simple interconnect testing) to be performed in a consistent and coordinated manner.

The overall structure of a basic 1149.4-conformant component is illustrated in Figure 6, which shows the main mandatory elements of the standard. In IEEE Std 1149.1, the main testability features are
a dedicated test access port (TAP), allowing test data to be passed to and from the circuit, and boundary modules associated with every digital function pin of the component, providing access to the core circuitry for the application of digital test stimuli and for the collection of digital test results. The 1149.4 extensions consist of analog boundary modules on every analog function pin, and optionally on other function pins, allowing access for analog test signals by way of an analog test access port (ATAP), consisting of two pins (AT1 and AT2), a test bus interface circuit (TBIC), and an internal analog test bus consisting of two lines (AB1 and AB2).

The boundary modules associated with the digital pins are identical to the boundary cells, or groups of boundary cells, as specified in IEEE Std. 1149.1; boundary modules on analog pins, which are forbidden in IEEE Std 1149.1, form the main subject of this standard, in which they are mandatory. It should be noted that each analog boundary module has associated with it a set of voltages \(V_H, V_L, \) and \(V_G\): these are defined on a pin-specific basis, so are not necessarily the same for each module.

Overall control of the testability structure rests with the test control circuitry, which consists of a TAP controller, an instruction register, and an instruction decoder.

Figure 6 : Structure of a basic (minimally configured) 1149.4 chip
4.2 TAP controller

4.2.1 State sequence

The TAP Controller, which is identical to that mandated in IEEE Std 1149.1, is a synchronous finite state machine whose state transition diagram is shown in Figure 7. The state transitions are determined by the value present on TMS at the time of a rising edge on TCK.

![State Transition Diagram](image)

Transitions are determined by the value of TMS, and take place on the rising edge of TCK.

Figure 7: TAP controller state transition diagram

4.2.2 Initialization

The TAP controller is required to enter the Test-Logic-Reset state at power-up either by use of an optional additional pin in the TAP (TRST*), or as a result of circuitry built into the test logic. Further description of the initialization requirements will be found in IEEE Std 1149.1.
4.2.3 Controller outputs

4.2.3.1 Specification

Rules

(a) The TAP controller shall generate signals to control the operation of the TBIC as defined in 6.3.

(b) The TAP controller shall generate signals to control the operation of the ABMs and associated circuitry as defined in 7.3.5.

(c) When the TAP controller is in the Test-Logic-Reset state, all function pins shall be isolated from the analog test buses, and from $V_H$, $V_L$, and $V_G$, irrespective of the state of the ABM control register bits.

(d) When the TAP controller is in the Test-Logic-Reset state, all ATAP pins shall be isolated from the analog test buses, and from $V_H$, $V_L$, and $V_{clamp}$, irrespective of the state of the TBIC control register bits.

4.2.3.2 Description

Control signals for routing data, reconfiguring the test circuitry, and exerting control over the TAP, the ATAP, and the TBIC, are derived partly from output logic of the TAP controller, and partly from the instruction register. In addition, the TBIC and each ABM contains an individual control register, so that its mode of operation can be individually controlled (see Clauses 6 and 7.3.) The instruction register, the ABM control registers, and the TBIC control register are all loaded through the TAP.

The precise set of signals required to control the test structure and boundary modules associated with digital function pins is not specified in IEEE Std 1149.1 except in terms of example implementations. Boundary modules are not required by the standard to support all instructions; the control signals needed will vary depending on the particular set of instructions supported by the individual component. These signals occur on either the rising or the falling edge of TCK in each controller state as specified in IEEE Std 1149.1.

All the example implementations of boundary-scan register cells described in IEEE Std 1149.1 use control signals ShiftDR and ClockDR; all those that incorporate the update register also use UpdateDR. Other control signals needed for the correct operation of the analog test structure will need to be generated by adding appropriate output logic to the TAP controller.
NOTE - Some output signals named in the example implementations of IEEE Std 1149.1, and also referred to in this standard, have the same names as some controller states. Throughout this standard, where this applies, control signals are shown in normal case (e.g., ShiftDR), and controller states are shown in italics (e.g., Shift-DR).

4.3  Analog test access port (ATAP)

4.3.1  Specification

Rules

(a) Each component shall contain an ATAP.

(b) The ATAP shall include two analog test pins, AT1 and AT2 (defined in Clause 6).

(c) AT1 and AT2 shall be dedicated pins (i.e., they shall not be used for any other purpose).

Permission

(d) The ATAP may contain two further analog test pins, AT1N and AT2N, to allow for the testing of differential input and/or output. In this case, AT1 and AT1N shall form one differential pair, and AT2 and AT2N shall form the other differential pair.

4.3.2  Description

The ATAP is an analog port that provides access for analog test signals. Dedicated connections are required to allow access to the full range of mandatory features of this standard. The ATAP is composed of a minimum of 1 analog input connection and 1 analog output connection. Optional additional analog lines can provide additional capability (e.g., differential stimulus and/or measurement: see 8.1.3). The definition and properties of the test bus interface circuit (TBIC) are specified in Clause 6.

4.4  Register architecture

The test register architecture, shown in Figure 8, is essentially identical to that defined in IEEE Std 1149.1. It is entirely digital, consisting essentially of a number of shift-register paths, connected in parallel with a common serial data input connected to TDI and a common serial data output connected to TDO. Control signals are required both for the transfer of data and for the choice of which of the alternative parallel paths is active: these signals are supplied, as shown in Figure 8, partly by the TAP controller and partly by the instruction decoder, interpreting the particular
instruction loaded into the instruction register.

The mandatory part of the test control architecture (as defined in IEEE Std 1149.1) consists of an instruction register together with at least two test data registers:

(i) a bypass register;

(ii) a boundary-scan register (as defined in Clause 7).

The test register structure of a component conformant with this standard differs from that of an 1149.1 component only in that additional shift-register stages are contained in the boundary-scan register. These additional stages consist of

(i) the control stages in the ABMs (as defined in 7.3);

(ii) the control stages in the TBIC (as defined in 6.3).

Figure 8: Test register structure

It should be noted that the order of the individual cells in the boundary-scan register can be chosen by the component manufacturer to suit layout convenience. It is not even necessary to keep the
control stages belonging to a single ABM or to the TBIC together in a single block, since the individual stages are identified by name.

An additional register (the device identification register) for part identification may be included, as well as any number of design-specific test data registers to give access to design-specific testability features. An example of a design-specific test register that could be included in a mixed-signal design would be an internal scan register used to give access to internal nodes of the core.

Depending on the style of implementation of the test logic defined by this standard, circuitry may be required to retime the signal passing through the output stage shown in Figure 8 to occur on the falling edge of TCK.
5 Instructions

5.1 General

5.1.1 Specification

Rule

(a) Each component shall provide a PROBE instruction. (See 5.3.4)

Permissions

(b) Additional instructions may be provided within the rules set out in this standard and in IEEE Std 1149.1.

(c) Any instruction code apart from all 1s and all 0s may be used to represent any instruction.

NOTE 1 - The instruction code consisting of all 1s is reserved for the BYPASS instruction.

NOTE 2 - The instruction code consisting of all 0s is reserved for the EXTEST instruction.

(d) Any instruction (including BYPASS and EXTEST) may be represented by more than one instruction code.

5.1.2 Description

An instruction is a bit-pattern that is loaded into the instruction register, and is then decoded by the instruction decoder. It has two major functions: it defines the set of test data registers that may operate while the instruction is selected, and it defines the serial test data register path that is used to shift data between TDI and TDO. The instruction set must include one instruction (PROBE) designed to support analog testing, together with the mandatory instructions from IEEE Std 1149.1 (BYPASS, SAMPLE/PRELOAD, and EXTEST - some with extended facilities). It may also include user-defined instructions as well as optional instructions defined in IEEE Std 1149.1.

The remainder of this clause lists all defined instructions. Instructions that derive from IEEE Std 1149.1 must satisfy the rules of IEEE Std 1149.1; the Rules, Recommendations, and Permissions listed herein are additional to the specifications contained in IEEE Std 1149.1. The instruction that is unique to this standard is fully specified and described; others are described in general terms for convenience.
5.2 Response of test logic to instructions

5.2.1 Specification

Rules

(a) Each component shall respond to the mandatory instructions of IEEE Std 1149.1 in accordance with the rules contained in IEEE Std 1149.1, together with any additional rules listed herein.

(b) Each component shall respond to the PROBE instruction in accordance with the rules in this standard.

(c) If a component provides any optional instructions defined in IEEE Std 1149.1, its response to those instructions shall be in accordance with the rules contained in IEEE Std 1149.1, together with any additional rules listed herein.

5.2.2 Description

The operation performed at any time by any particular DBM is determined in accordance with the rules of IEEE Std 1149.1. The operation performed at any time by any particular ABM is determined not only by the control signals supplied from the instruction decoder (which depend on the instruction currently loaded into the instruction register), but also by the control signals supplied by the TAP controller (which depend on the current state of the controller), and, depending on which instruction is selected, the values contained in the individual ABM control register.

The particular module design used in the test data registers (and the ABMs) will determine what control signals are required from the TAP controller and the instruction decoder. For the ABM design shown in Figure 23, for example, ShiftDR, ClockDR, and UpdateDR would be supplied by the TAP controller; Mode1 and Mode2 would be supplied from the instruction decoder.

Each instruction is represented by one or more instruction codes, and defines a particular test data register to be selected for serial connection between TDI and TDO. All instructions are defined in such a way that unselected test data registers have no effect on the operation of either the core circuitry or the selected test data register, unless specifically mandated in the instruction definition.

When implementing the instruction decoder, it is important to consider possible effects of decoding spikes when changing from one instruction to another (e.g., from BYPASS to SAMPLE/PRELOAD), so that transitory instruction selections are avoided.
5.3 Mandatory instructions

5.3.1 The BYPASS instruction

5.3.1.1 Specification

Rules

(a) When the BYPASS instruction is selected, all ATAP pins shall be isolated from the internal analog test buses and from all test voltage sources, irrespective of the state of the boundary register bits.

(b) When the BYPASS instruction is selected, all analog function pins shall be connected to the core circuit.

(c) When the BYPASS instruction is selected, all analog function pins shall be isolated from the internal and external analog test buses and from all test voltage sources, irrespective of the state of the boundary register bits.

5.3.1.2 Description

The BYPASS instruction selects the bypass register to be connected for serial access between TDI and TDO in the Shift-DR controller state. The BYPASS instruction can be selected by loading logic 1 into every stage of the instruction register (this coding is mandatory; optionally, other codes may also be designed to select BYPASS).

When the BYPASS instruction is selected, test data registers that can operate in either system or test mode perform their system function, and the operation of the test logic has no effect on the action of either the analog or the digital core circuitry.
5.3.2 The **SAMPLE/PRELOAD** instruction

5.3.2.1 Specification

Rules

(a) When the **SAMPLE/PRELOAD** instruction is selected, all ATAP pins shall be isolated from the internal analog test buses and from all test voltage sources, irrespective of the state of the boundary register bits.

(b) When the **SAMPLE/PRELOAD** instruction is selected, all analog function pins shall be connected to the core circuit.

(c) When the **SAMPLE/PRELOAD** instruction is selected, all analog function pins shall be isolated from the internal and external analog test buses and from all test voltage sources.

5.3.2.2 Description

This instruction has two functions. The first (SAMPLE) is to use the boundary-scan register to allow a snapshot to be taken of the data at the digital pins during normal operation. The snapshot is taken on the rising edge of TCK in the **Capture-DR** controller state, and can be examined serially by shifting through TDO.

A digitized snapshot of the (analog) signal on an analog pin will be captured in **SAMPLE/PRELOAD** by way of the one-bit digitizer in the ABM (see 7.3). The ability to monitor the analog signal itself is provided by the PROBE instruction (see 5.3.4).

The second function of this instruction (PRELOAD) is to allow an initial digital data pattern to be loaded into the latched parallel outputs of the boundary-scan register prior to the selection of another boundary-scan test operation. The loading is performed on the falling edge of TCK in the **Update-DR** controller state. During the PRELOAD phase, the operation of the core circuit and the flow of signals between the function pins and the core circuit are unaffected by the test logic.

In the same way, a digital data pattern can be specified for each ABM, by loading the appropriate values into its control register, which is part of the boundary-scan register.

NOTE - A future revision of IEEE Std 1149.1 may define SAMPLE and PRELOAD as separate instructions. In this case, the user could effectively re-merge them by using the same instruction code for both.
5.3.3 The \textit{EXTEST} instruction

5.3.3.1 Specification

Rule

(a) When the \textit{EXTEST} instruction is selected, each ABM shall be set so that the pin is disconnected from the core (i.e., the core disconnect switch shall be open).

5.3.3.2 Description

The \textit{EXTEST} instruction is used to test simple interconnect as in IEEE Std 1149.1 by applying logic levels to all pins. It is also used to test extended interconnect by allowing automatic test equipment (ATE) to make measurements of discrete components connected to the pins. The facilities incorporated into the boundary-scan test structure allow the ATE to apply analog test signals and monitor analog responses, and hence to obtain one of the major benefits of in-circuit testing without using physical probing. This instruction is the central feature of this standard: the principles underlying its use for analog measurements are outlined in Clause 8.

The \textit{EXTEST} instruction selects the boundary-scan register to be connected for serial access between TDI and TDO in the \textit{Shift-DR} controller state. While the \textit{EXTEST} instruction is selected, all function output pins (analog and digital) are isolated from the core. This allows the signals driven from system output pins to be completely defined by the data shifted into the corresponding boundary modules. Function input pins (analog and digital) are monitored by their boundary modules, and may be isolated from the core. If the facility to isolate input pins from the core during testing is not incorporated, the designer must ensure that signals appearing at an input pin during \textit{EXTEST} execution will not cause damage to the core, affect measurements on other pins, or be affected by core signals.

The \textit{EXTEST} instruction must be represented by the all 0s code, but may also be represented by other code(s).

\textbf{NOTE} - Because it is mandatory for the all 0s code to represent \textit{EXTEST}, a stuck-at-zero fault on TDI could then result in an unwanted selection of \textit{EXTEST}. Future revisions of IEEE Std 1149.1 may remove the requirement for all 0s to represent \textit{EXTEST}.
5.3.4 The **PROBE** instruction

5.3.4.1 Specification

Rules

(a) The **PROBE** instruction shall select the boundary-scan register to be connected for serial access between TDI and TDO in the *Shift-DR* controller state.

(b) When the **PROBE** instruction is selected, each DBM shall be set to allow core functions to propagate to and from the pins.

NOTE - This is similar to the requirements in **SAMPLE/PRELOAD** and **BYPASS**.

(c) When the **PROBE** instruction is selected, each ABM shall be set so that its pin is connected to the core (i.e., the core disconnect switch shall be closed).

(d) When the **PROBE** instruction is selected, one or both of the ATAP pins shall be connected to the corresponding internal analog test bus lines.

(e) When the **PROBE** instruction is selected, the internal analog test bus lines shall be connected to individual function pins as determined by the contents of the corresponding ABM control registers.

NOTE - The **PRELOAD** phase of the **SAMPLE/PRELOAD** instruction may be used to set up the contents of the ABM and TBIC control registers before the **PROBE** instruction is activated.

5.3.4.2 Description

The **PROBE** instruction allows analog pins to be monitored on AB2, and/or stimulated from AB1, while the component is operating in its normal mission configuration, with all function pins connected to the core.
5.4 Optional instructions

5.4.1 The INTEST instruction

5.4.1.1 Specification

Rules

(a) While the INTEST instruction is selected, all inputs to the digital part of the core shall be supplied by data stored in the boundary-scan register, except clocks, which may be allowed to free-run provided that the component can be single-stepped through the test sequence.

NOTE - The PRELOAD phase of the SAMPLE/PRELOAD instruction may be used to set up the contents of the boundary-scan register (including the ABM control registers) before the INTEST instruction is selected.

(b) While the INTEST instruction is selected, all analog pins shall be connected to the analog core.

NOTE - Because, in this mode of operation, much of the core is not isolated from the external circuitry, it may be necessary to control this external circuitry so as to avoid unwanted interference. Care should also be taken to ensure that the core itself does not generate unwanted interference.

(c) While the INTEST instruction is selected, any analog pin shall be capable of being connected to AB1.

NOTE - Because there is normally only one analog test bus input line available, only one analog stimulus can be supplied, although, if desired, the signal at AB1 could be applied to more than one input pin.

(d) While the INTEST instruction is selected, those inputs to the analog core that are normally supplied from the digital core shall receive data determined by the contents of the corresponding DBMs.

NOTE - The PRELOAD phase of the SAMPLE/PRELOAD instruction may be used to set up the contents of the DBMs before the INTEST instruction is activated.

(e) While the INTEST instruction is selected, any analog pin shall be capable of being monitored by AB2.

NOTE - The signal monitored by AB2 may be affected by more than one input. It may be necessary to apply external control to those inputs that are not being driven by AB1.
5.4.1.2 Description

The optional INTEST instruction is intended to allow testing of the core circuitry of a component while it is mounted on a printed circuit board. It selects the boundary-scan register to be connected for serial access between TDI and TDO in the Shift-DR controller state. Notice that, if INTEST is provided, there is a requirement (in IEEE Std 1149.1) for a DBM to be connected at each digital interface with the on-chip analog circuitry (see 7.2), as illustrated in Figure 9.

If the INTEST instruction is provided, it must permit the same test of the digital core as would be the case with a component conforming to IEEE Std 1149.1. In addition, the presence of the analog test structure permits some testing of the analog core.

In accordance with the rules of IEEE Std 1149.1, while the INTEST instruction is selected, all outputs from the digital part of the core are captured in the boundary-scan register on the rising edge of TCK in the Capture-DR controller state.

This together with rule (a) ensures that, as far as the digital part of the core is concerned, the operation of the instruction is exactly as described in IEEE Std 1149.1: every input to the digital core, whether normally supplied from a function pin or from the analog core, will have test data supplied by the boundary-scan register; every output from the digital core, whether normally connected to a function pin or to the analog core, will be captured in the boundary-scan register.

Figure 9: A component supporting INTEST (or RUNBIST) showing internal boundary modules

Figure 10 illustrates this part of the operation, as applied to the component shown in Figure 9. Notice that the DBMs mandatorily fitted between the digital and analog cores ensure that the analog core is completely isolated while the digital core is being tested.
Rules (b) to (e) are provided to support the testing of the analog core. If there is only one pair of analog test bus lines, as will normally be the case, only one analog input signal can be supplied and only one analog output can be fully monitored, although it might be possible to supplement this limited access by additional direct probing. It should also be noted that a one-bit digital representation of the voltage appearing at each analog pin will always be captured in the ABM control register on the rising edge of TCK in the Capture-DR controller state.

Figure 10 : Testing the digital core in INTEST

Figure 11 : Testing the analog core in INTEST
A typical analog core test, as it might be applied to the circuit of Figure 9, is illustrated in Figure 11. In this test, one of the analog outputs is being monitored through AT2 while one of the inputs is being supplied with an analog stimulus through AT1. Other inputs to the analog core include the signals normally supplied by the digital core and those coming from other analog function pins. During \textit{INTEST}, the digital signals will be supplied from the boundary-scan register (which will need to have appropriate data scanned in). Note 2 following rule (c) draws attention to the fact that all the analog pins (including the one being stimulated by way of AB1) are connected to the external circuitry on the board. This circuitry may have to be controlled to provide appropriate operating conditions, or to ensure that the input is rendered quiescent.

In addition to the analog output chosen for observation at AT2, digital test result data is captured in the DBMs in the analog/digital interface, and digitized results are captured in the control registers of all ABMs. This data is captured on the rising edge of TCK in the \textit{Capture-DR} controller state. Further test results for the same stimulus conditions could be obtained by repeating the test while monitoring each analog output in turn.

### 5.4.2 Device identification register instructions

These instructions make use of the optional identification register to allow internally stored codes to be read serially from TDO to identify the manufacturer, part number, and the version of the part. As far as the digital part is concerned, the behavior in response to these instructions of a component claiming conformance to this standard is identical to that of an IEEE Std 1149.1 component. Additional rules relating to the ATAP and the analog function pins are defined below.

#### 5.4.2.1 The \textit{IDCODE} instruction

#### 5.4.2.1.1 Specification

**Rules**

(a) When the \textit{IDCODE} instruction is selected, all ATAP pins shall be isolated from the analog test buses, irrespective of the state of the boundary register bits.

(b) When the \textit{IDCODE} instruction is selected, all analog function pins shall be connected to the core.

(c) When the \textit{IDCODE} instruction is selected, all analog function pins shall be isolated from the internal and external analog test buses and from all test voltage sources.
5.4.2.1.2 Description

If the device identification register is included in the design, then the IDCODE instruction must be supported. This instruction will then be loaded into the instruction register on the falling edge of TCK following entry into the Test-Logic-Reset controller state. The instruction can also be loaded serially through TDI while in the Shift-IR controller state.

When the IDCODE instruction is selected, the manufacturer’s identification code is loaded into the identification register on the rising edge of TCK following entry into the Capture-DR controller state, and can then be read serially through TDO.

5.4.2.2 The USERCODE instruction

5.4.2.2.1 Specification

Rules

(a) When the USERCODE instruction is selected, all ATAP pins shall be isolated from the analog test buses, irrespective of the state of the boundary register bits.

(b) When the USERCODE instruction is selected, all analog function pins shall be connected to the core.

(c) When the USERCODE instruction is selected, all analog function pins shall be isolated from the internal and external analog test buses and from all test voltage sources.

5.4.2.2.2 Description

If the device identification register is included in the design, and if the component is user-programmable such that the programming cannot otherwise be determined by the test logic, then the USERCODE instruction must be provided, and a user-programmed identification code must be included in the component. This code will, when the USERCODE instruction is selected, be loaded into the identification register on the rising edge of TCK following entry into the Capture-DR controller state, and can then be read serially through TDO.
5.4.3 The RUNBIST instruction

5.4.3.1 Specification

Rules

(a) The RUNBIST instruction shall be self-contained, and shall leave a single test result signature in the test data register selected by the RUNBIST instruction.

NOTE 1 - By self-contained is meant that no external stimulus is required apart from power and TAP signals.

NOTE 2 - The signature could be derived from a self-test conducted on the digital part of the core, while maintaining the analog part in a quiescent state; or the circuit could be designed to incorporate structures necessary to support analog stimulus generation and result collection (and digitization) so as to produce a composite signature.

NOTE 3 - The test data register will be selected by the designer. It could be the boundary-scan register.

(b) While RUNBIST is selected, analog function outputs shall behave in one of two ways.

(i) All output signals shall be defined by the data held in the boundary-scan register;

or

(ii) Every output signal shall be placed in the inactive CD state, which may be High-Z.

NOTE - These options are the same as those offered in IEEE Std 1149.1 for digital output pins.

(c) The choice of output behavior ((b) above) shall be the same for analog and digital pins.

Recommendation

(d) The test result should be a multi-bit signature.

NOTE - The purpose of a multi-bit signature is to allow a failed self-test to record diagnostic information rather than a simple GO/NOGO decision.

5.4.3.2 Description

The RUNBIST instruction is optional but in IEEE Std 1149.1 it is recommended that either INTEST or RUNBIST should be supported. If RUNBIST is supported, it is required to be self-contained, executing while in the Run-Test/Idle controller state. It is required to leave, in the test data register connected between TDI and TDO (which could be the boundary-scan register), a test result signature.
that is independent of any external signals that may be present at any of the pins. A mixed-signal circuit claiming conformance with this standard is required to provide exactly the same facilities.

5.4.4 The **CLAMP** instruction

5.4.4.1 Specification

Rules

(a) When the **CLAMP** instruction is selected, the state of all signals driven from analog function output pins shall be defined by the data held in the corresponding ABMs.

(b) While the **CLAMP** instruction is selected, the data held in the ABMs shall not change.

(c) When the **CLAMP** instruction is selected, the state of the AT1/2 pins shall be defined by the data held in the TBIC control register. (See 6.4).

5.4.4.2 Description

The optional **CLAMP** instruction selects the bypass register for connection between TDI and TDO in the *Shift-DR* controller state. While the **CLAMP** instruction is selected, the states of all signals driven from system output pins (analog and digital) are determined by the contents of the boundary modules. (This data can be previously inserted, e.g. by using the **PRELOAD** phase of the **SAMPLE/PRELOAD** instruction.)

5.4.5 The **HIGHZ** instruction

5.4.5.1 Specification

Rules

(a) When the **HIGHZ** instruction is selected, all analog function pins shall be disconnected from the core and from all test circuitry (i.e., all switches in the ABM, including the core disconnect switch, shall be open).

(b) When the **HIGHZ** instruction is selected, the AT1/2 pins shall be in the high impedance state, regardless of the data held in the TBIC control register. (See 6.2).

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5.4.5.2 Description

The optional \textit{HIGHZ} instruction selects the bypass register for connection between TDI and TDO in the \textit{Shift-DR} controller state. While the \textit{HIGHZ} instruction is selected, the component is put into a state in which all the function outputs are placed in an inactive drive (CD or high impedance) state. The ATAP pins are also isolated from the internal test bus lines (see NOTE 2 of Table 2).
6 The Test Bus Interface Circuit (TBIC)

6.1 General

The provision of facilities for the application and monitoring of analog test signals constitutes the main architectural feature of this standard. This clause describes the system of internal test buses to carry signals within the circuit, and the analog test bus interface circuit (TBIC), which controls the connections between the ATAP and the internal test buses. These elements provide a link between the system of external test buses that carry signals to and from the automatic test equipment (ATE) by way of pins in the ATAP (see 4.3), and the analog boundary modules (ABMs) within the component (see 7.3).

The simplest analog test structure that provides conformance with this standard consists of two pins in the ATAP (AT1 and AT2) and two internal bus lines (AB1 and AB2). The specification of this bus structure and its supporting TBIC is set out in 6.2 and 6.3. An optional extension that can be used for the testing of differential I/O is set out in 6.4 (although it should be noted that differential I/O can be tested using modified boundary modules instead of using this optional extension - see 7.4); the use of partitioned internal buses is described in 6.5.

6.2 Test bus and TBIC structure

6.2.1 Specification

Rules

(a) There shall be two internal analog test bus lines (AB1 and AB2).

(b) The connection of the internal test bus lines to the ATAP pins shall be controlled by a TBIC.

(c) During normal (non-test) operation of the component, the internal analog test bus lines (AB1 and AB2) shall be isolated from the ATAP.

(d) While the internal analog test bus lines are isolated from the ATAP, they shall have no effect on the operation of the component.

(e) There shall be a switchable connection between AT1 and AB1 such that current derived from an external source (e.g., an ATE) can be transmitted to AB1.
(f) There shall be a switchable connection between AB2 and AT2 such that a voltage
developed on AB2 can be monitored by an external measurement system (e.g., an ATE)
connected to AT2.

(g) There shall be a switchable connection between AT1 and AT2 via AB1 such that current
derived from an external source (e.g., an ATE) can be transmitted to AT2 without any other
paths being enabled.

(h) There shall be a switchable connection between AT1 and AT2 via AB2 such that a voltage
applied at AT1 can be monitored by an external measurement system (e.g., an ATE)
connected to AT2 without any other paths being enabled.

(i) It shall be possible to connect AB1 to AT1 whether or not AB2 is connected to AT2.

(j) It shall be possible to connect AB2 to AT2 whether or not AB1 is connected to AT1.

(k) It shall be possible to apply either of two voltage levels \(V_H\) or \(V_L\) to the external test bus
lines via the ATAP pins while they are isolated from their internal test bus lines.

(l) The TBIC shall be capable of monitoring one-bit digital representations of the voltages
appearing at each ATAP pin. The pin voltage is to be digitized with respect to a threshold
voltage \(V_{TH}\) (conceptual or actual) whose value lies in the range

\[
\left( \frac{V_H + V_L}{2} \right) \pm \left( \frac{V_H - V_L}{4} \right)
\]

NOTE 1 - The purpose of this digitization is to provide an unambiguous binary decision about the voltage at the
pin during simple interconnect testing. It needs to be borne in mind that when two pins driven to different logic
values are short-circuited, the voltage appearing on the combined net is likely to be at some value intermediate
between logic 0 and logic 1. The value for \(V_{TH}\), therefore, needs be chosen to be clearly different from any such
intermediate values.

NOTE 2 - A digitizer could in many cases be formed out of a simple logic gate, with its inherent threshold acting
as a conceptual \(V_{TH}\).

NOTE 3 - The monitored value is captured in the TBIC control register (see 6.3).

Recommendations

(m) Wherever possible, the switching structure should be implemented in such a way as to
support both current and voltage transmission.

NOTE - CMOS transmission gates inherently provide both current and voltage drive capability.

(n) Wherever possible, the switching structure should be implemented in such a way as to support bidirectional transmission.

NOTE - Optional design-specific features should be selected for use by design-specific instructions.

(o) Whenever an internal analog test bus line is disconnected from all ATAP pins, it should be connected to an internal source to ensure that it does not introduce noise into the core circuitry. This source \( V_{clamp} \) could be, but is not necessarily, GND.

Permissions

(p) Any internal test bus may be partitioned. (See 6.5.)

(q) Additional switches may be included to support additional instructions and modes of operation. Any such additional switches shall not interfere with the operation of any of the provisions of this standard or of IEEE Std 1149.1.

### 6.2.2 Description

The ATAP, TBIC, and internal and external analog test buses together provide the structure that supports parametric testing. In particular, measurements of impedance and other analog parameters can be derived from networks consisting of one or more discrete components mounted on a printed circuit board to form extended interconnect between two 1149.4-conformant components (see Figure 1 and Figure 2). The same structure also provides for parametric testing of the analog core of the component or (if appropriate internal test structures are included, and corresponding design-specific test instructions are supported) selected individual sub-circuits within the component.

During testing, an analog test input signal is supplied by the ATE to AT1, and analog test output is monitored at AT2; signals passing through AT1 and AT2 are distributed to the remainder of the component by way of a two-wire internal analog test bus (AB1 and AB2). From AB1 the test signal can be routed either to the core circuitry or through a function pin to the external circuitry; responses are directed to AB2 either from the core circuitry or from the external circuitry through a function pin.

At board level, external test bus lines will be distributed to the ATAP pins of every component...
conforming to this standard. Testing the integrity of these bus connections is therefore an important part of the board interconnect test: the facility to apply $V_H$ or $V_L$ to the ATAP pins, together with the requirement to capture digitized test values appearing at the pins, allows these connections to be tested in EXTEST along with all other simple interconnect.

The requirements described in the rules above imply that the TBIC consists of a set of ten conceptual switches and two digitizers as shown in Figure 12. Switches S1 - S8 represent the mandatory requirements, while S9 and S10 represent recommendation 6.2.1(o).

This switching structure allows each pin in the ATAP to be connected

- (i) to voltages $V_H$ and $V_L$, which act as logic values for interconnect testing (using switches S1 - S4);
- (ii) to each of the internal test bus lines (using switches S5 - S8);

Figure 12: TBIC switching architecture
and (iii) to the internal source $V_{\text{clamp}}$ (using switches S9 and S10). The value of $V_{\text{clamp}}$ would be chosen at the discretion of the manufacturer; its purpose is to hold the internal bus line at a constant value when not in use so as to avoid the noise problems that might arise if the lines were left to float.

The switching structure also allows the voltage appearing at each of the ATAP pins to be compared with the threshold voltage $V_{\text{TH}}$ to give one-bit digitized representations that can be captured into a register for subsequent inspection. Notice that, although Figure 12 shows each of $V_{\text{H}}, V_{\text{L}}, V_{\text{TH}}$ and $V_{\text{clamp}}$ as a single value associated with both ATAP pins, any or all of them could be made pin-specific.

One way of implementing the $V_{\text{H}}/V_{\text{L}}$ part of this structure (S1 - S4) is shown in Figure 13, in which a pair of logic drivers is controlled by three digital signals, $C$, $D_1$, and $D_2$. $C$ is an enable signal, such that if $C = 0$ both drivers are in a high-Z condition. If $C = 1$, each output is at $V_{\text{H}}$ or $V_{\text{L}}$ depending on whether the corresponding control ($D_1$ or $D_2$) is at logic 1 or logic 0 respectively. This is one implementation in which the values of $V_{\text{H}}$ and $V_{\text{L}}$ relating to the two pins are determined by different drivers, and so are not necessarily the same.

Table 1 shows a set of switch connection patterns that satisfy all the rules, together with recommendation 6.2.1(o).

The purpose of these switching patterns can be summarized as follows.

**P0:** This is the normal operating condition, when the internal bus lines (AB1 and AB2) are disconnected from the external bus lines (AT1 and AT2), and, if recommendation 6.2(o) is followed, connected to noise-suppressing dc source(s) ($V_{\text{clamp}}$). It also provides the high-Z condition that is needed for BYPASS, SAMPLE/PRELOAD, HIGH-Z, IDCODE, and USERCODE, and that can be used in other instructions.
Table 1: Switching patterns for TBIC (Figure 12)

<table>
<thead>
<tr>
<th>Pattern</th>
<th>Switch conditions</th>
<th>Connections and function</th>
</tr>
</thead>
<tbody>
<tr>
<td>P0</td>
<td>0 0 0 0 0 0 0 0 1 1</td>
<td>AB1/2 disconnected from AT1/2 and clamped. <strong>Mission mode, BYPASS, SAMPLE/PRELOAD, HIGHZ, IDCODE, USERCODE. Also high-Z in EXTEST.</strong></td>
</tr>
<tr>
<td>P1</td>
<td>0 0 0 0 0 1 0 0 0 0</td>
<td>AB1 connected to AT1 and/or AB2 connected to AT2; disconnected bus clamped. <strong>PROBE, INTEST.</strong> Extended interconnect testing in EXTEST.</td>
</tr>
<tr>
<td>P2</td>
<td>0 0 0 0 1 0 0 0 0 1</td>
<td></td>
</tr>
<tr>
<td>P3</td>
<td>0 0 0 0 1 1 0 0 0 0</td>
<td></td>
</tr>
<tr>
<td>P4</td>
<td>0 0 1 1 0 0 0 0 1 1</td>
<td>AT1/2 = 00 Logic signals applied to AT1/2. Internal buses clamped. <strong>Simple interconnect testing (EXTEST).</strong></td>
</tr>
<tr>
<td>P5</td>
<td>0 1 1 0 0 0 0 0 1 1</td>
<td>AT1/2 = 01</td>
</tr>
<tr>
<td>P6</td>
<td>1 0 0 1 0 0 0 0 1 1</td>
<td>AT1/2 =10</td>
</tr>
<tr>
<td>P7</td>
<td>1 1 0 0 0 0 0 0 1 1</td>
<td>AT1/2 = 11</td>
</tr>
<tr>
<td>P8</td>
<td>0 0 1 1 0 0 0 1 1 0</td>
<td>AT1 connected to AT2 via internal buses. <strong>Characterization (in EXTEST).</strong></td>
</tr>
<tr>
<td>P9</td>
<td>0 0 1 1 0 1 0 0 1 1</td>
<td></td>
</tr>
</tbody>
</table>

P1-3: These are the main testing conditions, in which either or both of the external bus lines are connected to the internal bus lines, and internal bus lines that are disconnected from the ATAP pins are connected to \( V_{clamp} \). They are used for the **PROBE** and **INTEST** instructions, when the function pin is connected to the core, and for analog measurements in the **EXTEST** instruction, when the function pin is isolated from the core.

P4-7: These connection patterns apply logic signals (\( V_H \) or \( V_L \)) to the ATAP pins while the
internal bus lines are clamped for noise-suppression. They are used in \textit{EXTEST} to check the external bus lines as part of the board-level interconnect.

Table 2 : TBIC switching assignments for defined instructions

<table>
<thead>
<tr>
<th>Code $C_a/C_o$ $D_1/D_2$ (See Figure 14)</th>
<th>Instruction</th>
<th>Code $C_a/C_o$ $D_1/D_2$ (See Figure 14)</th>
<th>Instruction</th>
</tr>
</thead>
<tbody>
<tr>
<td>\textit{EXTEST}, \textit{CLAMP}, \textit{RUNBIST}</td>
<td>\textit{PROBE}, \textit{INTEST}</td>
<td>\textit{EXTEST}, \textit{CLAMP}, \textit{RUNBIST}</td>
<td>\textit{PROBE}, \textit{INTEST}</td>
</tr>
<tr>
<td>0000</td>
<td>P0</td>
<td>1000</td>
<td>P0</td>
</tr>
<tr>
<td>0001</td>
<td>P1</td>
<td>1001</td>
<td>P8</td>
</tr>
<tr>
<td>0010</td>
<td>P2</td>
<td>1010</td>
<td>P9</td>
</tr>
<tr>
<td>0011</td>
<td>P3</td>
<td>1011</td>
<td>*</td>
</tr>
<tr>
<td>0100</td>
<td>P4</td>
<td>1100</td>
<td>*</td>
</tr>
<tr>
<td>0101</td>
<td>P5</td>
<td>1101</td>
<td>*</td>
</tr>
<tr>
<td>0110</td>
<td>P6</td>
<td>1110</td>
<td>*</td>
</tr>
<tr>
<td>0111</td>
<td>P7</td>
<td>1111</td>
<td>*</td>
</tr>
</tbody>
</table>

\textbf{NOTE 1} - \textit{RUNBIST} will select the same switching patterns as \textit{CLAMP} if the option in 5.4.3.1(b)(i) is exercised.

\textbf{NOTE 2} - All other defined instructions (\textit{BYPASS}, \textit{SAMPLE/PRELOAD}, \textit{HIGHZ}, \textit{IDCODE}, and \textit{USERCODE}), as well as normal mission function require P0 for all codes.

\textbf{NOTE 3} - Code bits are CALIBRATE ($C_a$), CONTROL ($C_o$), DATA1 ($D_1$), and DATA2 ($D_2$); instructions are represented by mode bits supplied by the instruction decoder.

\textbf{NOTE 4} - Entries marked with an asterisk are undefined in this issue of the standard. The effects produced by the corresponding codes would depend on the particular implementation. In general, it would not be good practice to allow such codes to be entered by the test program, since they could be assigned specific functions in future revisions of the standard.

\textbf{NOTE 5} - The assignments of switching patterns to codes for user-defined instructions is not restricted. Such assignments would be selected when the appropriate user-defined instruction code is decoded by the instruction decoder.
P8-9: These patterns are used to permit the measurement of the characteristics of the test buses (and internal switches) by applying test signals at the ATAP, passing them through AB1 or AB2, and monitoring the resulting output at the ATAP without the signal passing through any other internal circuitry.

Additional connection patterns could be provided to support optional instructions; additional switches may also be fitted to increase flexibility, but the consequential effects on parasitic loading of the test buses will need to be taken into account. These patterns will be invoked as appropriate to serve the needs of the various instructions, as shown in Table 2.

6.3 Control of the TBIC

The TBIC consists of the switching structure (Figure 12) designed in accordance with the rules in 6.2.1, together with a control circuit that allows the various connection patterns (Table 2) to be selected.

6.3.1 Specification

Rules

(a) The TBIC shall contain a control register and an update register.

(b) The control register shall consist of a shift register with four stages identified by the labels CALIBRATE, CONTROL, DATA1, and DATA2.

(c) The control register shall form part of the boundary-scan register.

(d) The DATA1 and DATA2 stages of the control register shall capture the results of the digitizations of the pin voltages at AT1 and AT2 respectively on the rising edge of TCK while the TAP controller is in the Capture-DR state.

(e) The update register shall be parallel loaded from the control register and any necessary combinational logic in response to the falling edge of TCK while the TAP controller is in the Update-DR state, such that serial shifting in the control register has no effect on the state of the switches.

(f) The control circuit shall be designed to support the operating patterns shown in Table 1 and Table 2.
Permissions

(g) The CALIBRATE and CONTROL stages of the control register may be used at the designer's discretion to capture other internal states on the rising edge of TCK while the TAP controller is in the Capture-DR state, provided that no rules of this standard are violated.

(h) The positioning of individual stages of the control register within the boundary-scan register is entirely at the discretion of the manufacturer.

(i) Additional switching pattern assignments may be incorporated at the manufacturer’s discretion to support user-defined instructions.

6.3.2 Description

One possible implementation of a TBIC controller is shown in Figure 14, which provides the control needed for the TBIC of Figure 12 (including the optional (recommended) switches S9 and S10), and supports the switch connection patterns in Table 2. It should be noted that it is the designer’s responsibility to ensure that any particular realization of a TBIC will perform correctly according to the rules when implemented within a particular fabrication facility. It may be necessary, for example, to control the skew of the UpdateDR signal.

Because the TBIC control register is included as part of the boundary-scan register, appropriate control codes can be entered serially in response to rising edges on TCK while the TAP controller is in Shift-DR, at the same time that the boundary modules are being loaded with data.

The control signals for the individual switches are derived by the control logic from the contents of the update register together with a set of Mode signals, which would be supplied by the instruction decoder. In the circuit of Figure 14, the mode signals used (Mode1 and Mode2) are those defined in Table 3, which are sufficient to support all the mandatory and optional instructions defined in IEEE Std 1149.1 and this standard. If additional user-defined instructions are supported, additional mode signals will probably need to be generated by the instruction decoder to allow the appropriate switch patterns to be selected.
Figure 14: TBIC - Example implementation of the control structure

Table 3: Possible mode signal assignments to identify instructions

<table>
<thead>
<tr>
<th>Instruction</th>
<th>Mode1</th>
<th>Mode2</th>
</tr>
</thead>
<tbody>
<tr>
<td>EXTEST, CLAMP, RUNBIST</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>PROBE, INTEST</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>HIGHZ</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>Other Instructions</td>
<td>0</td>
<td>0</td>
</tr>
</tbody>
</table>

NOTE - Other instructions include normal mission function as well as BYPASS, SAMPLE/PRELOAD, IDCODE, and USERCODE.
The detailed design of the TBIC therefore requires that versions of Tables 1, 2, and 3 must first be prepared, taking into account the instructions that are to be supported (i.e., mandatory + optional + user-defined). Table 1 could include additional switching patterns for user-defined purposes; Table 2 could include additional columns (for user-defined instructions) and/or could use different codings to select the patterns; Table 3 could need additional mode signals to identify instructions and/or could code them differently.

To design the control logic needed (see Figure 14) to control a particular switch, it is necessary to identify (from Table 1) which patterns require that switch to be closed. Table 2 then shows which codings under which instructions select those patterns, and Table 3 shows the appropriate mode signals that identify the instructions.

The procedure can be illustrated using the tables as they are (i.e., implementing a TBIC for a component supporting all defined instructions (mandatory and optional) but no user-defined instructions) and finding the logic to drive switch S5. Note that in the equations the control signal for switch SN is denoted by \( S_N \), and that the code and mode bits are denoted by \( \text{CALIBRATE} = C_a; \) \( \text{CONTROL} = C_o; \) \( \text{DATA1} = D_1; \) \( \text{DATA2} = D_2; \) \( \text{Mode1} = M_1; \) \( \text{Mode2} = M_2. \)

1. From Table 1 we find that S5 is required to be closed for P2, P3, and P9.

2. From Table 2 we find that P2 is required in EXTEST, CLAMP, RUNBIST, PROBE, and INTEST for code \( C_a C_o D_1 D_2 = 0010; \) P3 is required in EXTEST, CLAMP, RUNBIST, PROBE, and INTEST for code \( C_a C_o D_1 D_2 = 0011; \) and P9 is required in EXTEST, CLAMP, and RUNBIST for code \( C_a C_o D_1 D_2 = 1010. \)

3. From Table 3 we find that the group of instructions EXTEST, CLAMP, and RUNBIST is represented by \( M_1 M_2 = 11, \) and that the group PROBE and INTEST is represented by \( M_1 M_2 = 01. \)

4. Putting these together we then get

\[
S_5 = \overline{C_a} \overline{C_o} D_1 \overline{D_2} M_1 M_2 \\
+ \overline{C_a} \overline{C_o} D_1 D_2 \overline{M_1} M_2 \\
+ \overline{C_a} \overline{C_o} D_1 D_2 M_1 M_2 \\
+ C_a \overline{C_o} D_1 \overline{D_2} M_1 M_2 \\
+ C_a \overline{C_o} D_1 D_2 \overline{M_1} M_2
\]

which can be simplified to
The full set of logic equations for the control logic in Figure 14 then becomes

\[
S_5 = \overline{C_o} D_1 M_2 \left( \overline{C_a} + \overline{D_2} M_1 \right)
\]

The other control signals used in the circuit of Figure 14 are UpdateDR, ShiftDR, and ClockDR, which would be generated by the TAP controller (as in the example TAP controller implementation shown in IEEE Std 1149.1). These signals are used to control the entry into the TBIC registers of data supplied serially through TDI, the capture of digitized data, the transfer of data to the Update Register, and the serial inspection of data through TDO.

The results of interconnect tests on AT1 and AT2 are captured from the comparators at the bottom of Figure 14 (these are the same comparators as shown in Figure 12); also shown in Figure 14 are the optional multiplexers that can be included at the inputs of the CALIBRATE and CONTROL stages of the control register to capture the states of any two additional internal nodes.

It should be noted that the AT1 and AT2 pins are disconnected from the internal circuitry (high-Z) during mission mode and when the component is in Test-Logic-Reset. To prevent these buses from causing undesired signal coupling, users will need to make provision on the board for clamping the buses. Possibilities include high impedance resistors (> 1 MΩ), suitably controlled 3-state drivers, or temporary jumper wires.
6.4 Differential I/O

6.4.1 Specification

Rules

(a) If additional ATAP pins (AT1N and AT2N) are provided in accordance with Permission 4.3.1(d), corresponding additional internal analog test bus lines (AB1N and AB2N) shall be provided.

(b) The additional pair of ATAP pins shall be connected to its corresponding pair of internal bus lines by a second TBIC that conforms to the rules set out in 6.2 and 6.3.

6.4.2 Description

If some of the function pins carry differential input or output signals, the manufacturer may choose to include additional test structures to provide for differential testing, or may choose to omit the additional structure and accept a reduced level of test function.

The optional additional structure consists of two additional pins in the ATAP (AT1N and AT2N), and two corresponding additional internal buses (AB1N and AB2N). The control of this additional structure is exercised by an additional TBIC, identical to that shown in Figure 12. The options with regard to boundary modules are described in 7.4, and the options with regard to test methodologies are described in 8.1.2 and 8.1.3.

6.5 Partitioned internal test bus structure

In the simplest form of the test bus structure that has been described so far, a two-wire internal test bus will be distributed to all analog pins in the component. There are some designs (particularly those with multiple power supply voltages) for which this structure could lead to performance problems because of cross-talk, leakage, feedback, or loading. One way of alleviating some of these problems is to partition the internal test buses.

6.5.1 Switching

A general partitioning scheme consists of a two-pin ATAP (AT1/2) and \( n \) partitions each consisting of a pair of internal buses (AB1\( n \) and AB2\( n \)).
6.5.1.1 Specification

Rules

(a) The TBIC switching structure shall consist of

(i) a single set of four switches and two digitizers connected to AT1/2;

(ii) for each partition \( n (n = a, b, \ldots) \), a set of four switches connected between AT1/2 and AB1/2n.

NOTE - The implementation of 6.2.1(o) may require the inclusion of two further switches \( S9/10_n \) in each partition.

(b) The capabilities and functioning of the switching structure shall conform to the rules, recommendations, and permissions laid down in 6.2.1.

6.5.1.2 Description

The switching patterns required for logic testing and for control of partition \( a \) remain as set out in Table 1, with switches \( S5a - S10a \) replacing S5 - 10. Each additional partition \( n \), consisting of switches \( S5n - S10n \), will need to support switching patterns \( P0n - P3n \) and \( P8n - P9n \), as set out in Table 4.

Figure 15 : TBIC switching structure for partitioned internal buses
Table 4: TBIC switching patterns for bus partition $n$ (Figure 15)

<table>
<thead>
<tr>
<th>Pattern</th>
<th>Switch conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>5n</td>
</tr>
<tr>
<td>P0$n$</td>
<td>0</td>
</tr>
<tr>
<td>P1$n$</td>
<td>0</td>
</tr>
<tr>
<td>P2$n$</td>
<td>1</td>
</tr>
<tr>
<td>P3$n$</td>
<td>1</td>
</tr>
<tr>
<td>P8$n$</td>
<td>0</td>
</tr>
<tr>
<td>P9$n$</td>
<td>1</td>
</tr>
</tbody>
</table>

These patterns will be invoked as appropriate to serve the needs of the various instructions, as shown in Table 5, in which all defined instructions are assumed to be supported.

Table 5: TBIC partition $n$ assignments for defined instructions

<table>
<thead>
<tr>
<th>Code $C_a/D_{1n}/D_{2n}$ (see Figure 16)</th>
<th>Instruction</th>
<th>Code $C_a/D_{1n}/D_{2n}$ (see Figure 16)</th>
<th>Instruction</th>
</tr>
</thead>
<tbody>
<tr>
<td>EXTEST, CLAMP, RUNBIST</td>
<td>PROBE, INTTEST.</td>
<td>EXTEST, CLAMP, RUNBIST</td>
<td>PROBE, INTTEST.</td>
</tr>
<tr>
<td>000</td>
<td>P0$n$</td>
<td>100</td>
<td>P0$n$</td>
</tr>
<tr>
<td></td>
<td>P0$n$</td>
<td></td>
<td>*</td>
</tr>
<tr>
<td>001</td>
<td>P1$n$</td>
<td>101</td>
<td>P8$n$</td>
</tr>
<tr>
<td></td>
<td>P1$n$</td>
<td></td>
<td>*</td>
</tr>
<tr>
<td>010</td>
<td>P2$n$</td>
<td>110</td>
<td>P9$n$</td>
</tr>
<tr>
<td></td>
<td>P2$n$</td>
<td></td>
<td>*</td>
</tr>
<tr>
<td>011</td>
<td>P3$n$</td>
<td>111</td>
<td>*</td>
</tr>
</tbody>
</table>

NOTE - These assignments are valid only when $C_o = 0$: when $C_o = 1$, switching patterns P4 - P7 are being used to apply EXTEST to AT1/2.
6.5.2 Control

6.5.2.1 Specification

Rules

(a) For a component whose internal test bus structure has $n$ partitions, the TBIC shall contain a control register and an update register, the structure and functioning of which (e.g., the mechanism for the transfer of data through the control register, and from the control register to the update register) shall be identical to that of the single partition case, as laid down in 6.3.

(b) The TBIC control and update registers shall consist of a base section together with $(n - 1)$ extensions.

(c) The base section of the TBIC shall consist of four stages labelled CALIBRATE, CONTROL, DATA1, and DATA2, and the contents of these stages shall control the interconnect test facility (switches S1 - S4 in Figure 15) and partition $a$ (switches S5a - S10a in Figure 15). The function and performance of the base section of the TBIC shall conform to the rules laid down in 6.2.

(d) Each additional partition shall be associated with a two-bit extension to the TBIC; the bits associated with partition $n$ being labelled DATA1$n$ and DATA2$n$.

(e) The control register stages of the extension(s) to the TBIC shall be incorporated into the boundary-scan register.

(f) The contents of the TBIC extension, together with the contents of the CALIBRATE and CONTROL stages of the base section, shall provide the switching patterns P0$n$ - P3$n$ and P8$n$ - P9$n$ as defined in Table 4.

(g) The control circuit associated with extension $n$ shall be designed to produce the operating patterns required by the instruction set (e.g., Table 5).

Permission

(h) The DATA1$n$ and DATA2$n$ stages of the TBIC extension may be used at the designer's discretion to capture internal states on the rising edge of TCK while the TAP controller is in the Capture-DR state, provided that no rules of this standard are violated.
The TBIC extension may be incorporated into the boundary-scan register in any position.

6.5.2.2 Description

The overall structure of the TBIC is illustrated in Figure 16. The four stages on the left represent the base section, and the control logic for this section would obey the same equations as for the unpartitioned case (see 6.3.2).

![Diagram of control logic](image)

Figure 16: Control of a partitioned bus structure

The control logic for partition $n$ in Figure 16 will satisfy the switching pattern requirements of Table 5 if it implements the following equations, derived from Tables 4 and 5 in the same way as the equations in 6.3.2.

$$
S_{5n} = \overline{C_a} D_1 n M_2 (\overline{C_a} + \overline{D_2 a} M_1 )
$$

$$
S_{6n} = \overline{C_a} D_2 a M_2 (\overline{C_a} + \overline{D_1 n} M_1 )
$$

$$
S_{7n} = \overline{C_a} C_a \overline{D_1 n} D_2 n M_1 M_2
$$

$$
S_{8n} = \overline{C_a} C_a D_1 n \overline{D_2 n} M_1 M_2
$$

$$
S_{9n} = \overline{S_{5n}}
$$

$$
S_{10n} = \overline{S_{6n}}
$$
7 The Boundary-Scan Register

7.1 Structure

7.1.1 Introduction

Each function pin has associated with it a boundary module, containing one or more register stages. The boundary-scan register consists of the concatenation of register stages from each of the boundary modules, together with the TBIC control register, into a single shift register.

The analog boundary modules (ABMs) are mixed-signal elements, in which a digital control register determines the flow of analog and digital signals into and out of the analog function pins. The control registers in the ABMs are connected as part of the boundary-scan register.

The digital boundary modules (DBMs) (termed boundary-scan register cells in IEEE Std 1149.1) can be of many different forms. Each DBM is a logic element contributing one or more stages to the boundary-scan register, which can be loaded serially from the TAP, or can be loaded in parallel, capturing the value being delivered at an input pin by the off-chip circuitry, or being produced at an output from the core. A control-and-observe DBM is one with parallel output capability; an observe-only DBM is one without parallel output capability. The distinction between these two types of DBM is important when dealing with differential I/O.

7.1.2 Specification

Rule

(a) The boundary-scan register shall consist of a concatenation of the shift register stages of all the DBMs, the control registers of all the ABMs, and the control register(s) of the TBIC(s).

NOTE - The individual stages may be concatenated in any order.

7.1.3 Description

The boundary-scan register allows signals to be applied to the function pins without having to pass through the core circuitry, and optionally allows signals to be applied to the core circuitry without having to pass these signals in through the function pins. These signals are applied using serial digital access to the boundary-scan register, and analog stimulus access to the AT1 pin. For a component conforming to this standard, there are two forms that the boundary-scan register can take, illustrated...
in Figure 17.

![Figure 17: Alternative forms of boundary scan register](image)

The simplest form of boundary-scan register is shown in Figure 17(a), where the only boundary modules are those associated with the function pins (both analog and digital). Additional DBMs may also be fitted on the digital side of the interface(s) between the analog and digital cores of a mixed-signal component: these internal modules must be incorporated if the component supports INTEST or RUNBIST, and may optionally be included even if the component does not support INTEST or RUNBIST. If internal modules at the analog/digital interface are implemented, they will be included in the boundary-scan register, as illustrated in Figure 17(b).

### 7.2 Digital boundary modules (DBMs)

#### 7.2.1 Specification

Rules

(a) Either a DBM or an ABM shall be connected to each digital function pin.

NOTE 1 - This rule applies equally to digital differential function pins, notwithstanding the rules in IEEE Std 1149.1.

NOTE 2 - In all other respects, DBMs must conform to the rules governing boundary-scan cells as set out in IEEE Std 1149.1; ABMs must conform to the rules set out in 7.3.
(b) Where it is possible for the pair of output signals from a digital differential driver to be used independently, the two output pins shall each be connected to a control-and-observe DBM.

(c) Where it is not possible for the pair of output signals from a digital differential driver to be used independently, the two output pins shall each be connected to an observe-only DBM.

(d) Where it is not possible for the pair of output signals from a digital differential driver to be used independently, the driver input shall be connected to an observe-and-control DBM.

(e) A DBM shall be connected to the output of any digital differential receiver whose inputs are driven from function pins.

(f) If \textit{INTEST} or \textit{RUNBIST} is supported, a DBM shall be connected at the digital interface with on-chip analog circuitry.

\textbf{NOTE} - Notwithstanding the rules contained in IEEE Std 1149.1, DBMs need not be fitted at the digital interface with on-chip analog circuitry if neither \textit{INTEST} nor \textit{RUNBIST} is supported.

Recommendation

(g) Where it is possible for the pair of output signals from a digital differential driver to be used independently, the driver input should be connected to a DBM.

Permissions

(h) The DBMs connected at the inputs of a digital differential receiver may be either control-and-observe or observe-only.

\textbf{NOTE} - If control-and-observe DBMs are used, this will require a user-defined instruction to make full use of the facilities.

(i) If a DBM is connected at the input of a digital differential driver whose outputs can be used independently, it may be either control-and-observe or observe-only.

\textbf{NOTE} - If a control-and-observe DBM is used, this will require a user-defined instruction to make full use of the facilities.

(j) The DBM connected at the output of a digital differential receiver may be either control-and-observe or observe-only.
NOTE - If a control-and-observe DBM is used, this will require a user-defined instruction to make full use of the facilities.

(k) A DBM may be connected at the digital interface with on-chip analog circuitry if neither INTEST nor RUNBIST is supported.

7.2.2 Description

The specification of the boundary-scan register in IEEE Std 1149.1 is confined to detailing aspects of function, and the implementations contained in it are illustrative only. There is no requirement on any individual component to support all instructions. A very detailed discussion of possible options is contained in IEEE Std 1149.1.

The rules for digital differential I/O in this standard differ slightly from those in the 1993 edition of IEEE Std 1149.1, particularly with regard to the rules for placement of DBMs and the options relating to the types of DBM to be used.

Figure 18 shows possible placements for DBMs associated with digital differential I/O. It should be noted that a control-and-observe DBM places circuitry in the pathway between pin and core, and that this pathway is disabled in some states of the TAP controller when some instructions are selected. An observe-only DBM, on the other hand, is non-invasive: the pathway between core and pin is always closed.

![Figure 18: Placement of DBMs at differential I/Os](image)

Differential input pins must be connected to DBMs (Rule (a)); these may be observe-only DBMs, or they may be control-and-observe DBMs (Permission (n)), although in the latter case the control function cannot be available in EXTEST or INTEST, so that a user-defined instruction would be
required to provide access to it. A third DBM is required to capture the signal at the output of the receiver; this can be either observe-only or control-and-observe (Rule (e) and Permission (j)).

For differential output pins, the placement of DBMs depends on the design of the differential driver:

(i) Where it is possible to inject test control such that the output signals can be controlled independently to either of two logic states, the output pins must be connected to control-and-observe DBMs (Rule (b)). This provides the highest degree of controllability and consequent test coverage. It also ensures testability of board-level interconnections where one of the output signals from a pair is used to drive a single-ended input pin on another component. Optionally, a third DBM, which can be either observe-only or control-and-observe, may be provided at the input to the differential driver (Recommendation (g) and Permission (i)). Again the use of a control-and-observe DBM would require a user-defined instruction: in this case, the facility would be used to control the differential driver from its single-ended input to allow test control of the signal when the differential signaling is required for proper transmission.

(ii) Where such control is not possible (i.e., the signals are always, in test and function modes, inherently driven to opposing states), three DBMs must be provided for each differential driver. In addition to two observe-only DBMs at the output pins, a control-and-observe DBM must be provided at the driver input (Rules (c) and (d)).

Permission (k) allows the incorporation of test structures to test on-chip ADCs and DACs.

Fitting an ABM rather than a DBM at a particular digital output pin allows the designer to take advantage of the analog test features provided by this standard so that (e.g.) pull-up resistors on bus lines can be measured. The use of this Permission effectively requires the designer to regard the digital pin as though it were analog, and to attach to it an ABM, complete with its four-bit control and update registers (see 7.3).

7.3 Analog boundary modules (ABMs)

7.3.1 Specification

Rules

(a) An ABM shall be connected to each analog function pin.

NOTE 1 - This rule applies notwithstanding the provisions of IEEE Std 1149.1, in which boundary modules on
analog pins are forbidden.

NOTE 2 - The ABMs attached to differential pins are subject to additional rules (see 7.4).

(b) Each ABM shall be designed with a “core disconnect” facility.

NOTE 1 - Core disconnect is intended to allow the pin to be effectively isolated from all internal ac and dc sources, and to allow it to be driven externally without adversely affecting the core circuitry. When this facility is invoked, the pin is said to be in the CD state.

NOTE 2 - The most straightforward way of satisfying this rule is to include a conceptual switch between the pin and the core. The core disconnect facility may, in many cases, be integrated into the core circuitry.

(c) The ABM shall be designed so that the pin is capable of being connected to neither, either or both of two internal analog test bus lines.

NOTE 1 - The two test bus lines shall be AB1 and AB2 except when additional analog test bus lines are supplied for differential stimulus and/or measurements (see 6.4), or when the internal bus lines are partitioned (see 6.5).

NOTE 2 - When additional analog test bus lines are supplied for differential stimulus and/or measurements (see 6.4), an ABM attached to a positive input or output shall be associated with AB1 and AB2, while an ABM attached to a negative input or output shall be associated with AB1N and AB2N.

(d) The ABM shall be capable of transmitting current received from AB1 through its function pin to an external circuit.

(e) The ABM shall be capable of transmitting to AB2 the voltage appearing on its function pin.

(f) The ABM shall be capable of monitoring a one-bit digital representation of the voltage appearing at the pin. The pin voltage is to be digitized with respect to a voltage $V_{TH}$ (conceptual or actual) whose value lies in the range

$$\left(\frac{V_H + V_L}{2}\right) \pm \left(\frac{V_H - V_L}{4}\right)$$

NOTE - The choice of $V_{TH}$ in this case is subject to the same conditions as expressed in the notes attached to rule 6.2.1(l).

(g) The ABM shall be designed so that the pin is capable of delivering either of two voltage levels ($V_H$ or $V_L$) to the external circuitry.
NOTE 1 - The values of $V_H$ and $V_L$ are pin-specific: they could each be the same on all pins, but are not necessarily so.

NOTE 2 - $V_H$ and $V_L$ are used as logic levels when testing simple interconnect in EXTEST. For an analog pin, the values used for logic 0 and logic 1 shall be the minimum and maximum values attainable at the pin in its normal functional mode.

NOTE 3 - To facilitate network measurements, the requirement to be able to drive $V_H$ and $V_L$ out of the pin holds for input as well as output pins.

(h) The ABM shall be designed so that the pin can be connected to one reference quality voltage ($V_G$).

NOTE - $V_G$ must be one of the voltages supplied externally to a pin of the component. This would normally be one of the power rail voltages (including GND), but could alternatively be a bias or other reference supply provided that it is capable of sourcing/sinking the required currents.

Recommendations

(i) For an output pin, $V_H$ and $V_L$ should be supplied by the functional output driver.

7.3.2 Description

The ABM is at the heart of the standard framework for mixed-signal test. Figure 19 shows a functional schematic of the module, consisting of six conceptual switches connected to the pin.

SB1 and SB2 are provided to satisfy Rule 7.3.1(c), allowing the analog buses to be used as “virtual probes”, so that AT1 and/or AT2 can be connected to any component pin without the need for physical probing. The use of this structure to perform component measurements is described in 8.2 and 8.3.

The inclusion of the digitizer, together with its threshold voltage $V_{TH}$, satisfies Rule 7.3.1(f), and allows the level actually appearing at the pin to be monitored; this facilitates the detection of bridging faults in the interconnect, provided that the value of $V_{TH}$ is chosen so that likely values under fault conditions are unambiguously coded.

SH and SL provide for Rule 7.3.1(g), with $V_H$ and $V_L$ corresponding to the two voltage levels. These can be regarded as logic levels, and allow simple interconnect testing on analog pins to take place at the same time, and using the same methods, as digital interconnect testing.

SG is provided to satisfy Rule 7.3.1(h), by allowing the pin to be connected to the reference quality
voltage $V_G$. The implementation of this provision is discussed in detail in 8.2.2.

SD is the core disconnect facility (Rule 7.3.1(b)), allowing the pin to be isolated from the core circuitry while external testing is taking place. As far as input pins are concerned, the core disconnect is intended to ensure that the analog core does not respond noisily or unsafely to test signals. This might require additional circuitry to be associated with this switch function, such as is shown in Figure 20.

If a separate physical switch in the input data path is unacceptable in terms of its impact on normal functional performance, the switch function represented by SD may be omitted; it is then the
responsibility of the manufacturer to ensure that no part of the core circuitry will be adversely affected by any signal that could be presented at the pin by the test circuitry.

For output pins, the function represented by SD could, in many cases, be integrated into the core circuitry - e.g., the pin driver circuit in an analog functional output could be replaced by a 3-state buffer circuit, as shown in Figure 21, in which the driver has been designed so that it is able to go to a core disconnect output state or to provide one of two fixed (not input-dependant) outputs under the control of logic input signals SD, SH, and SL, where

\[
\begin{align*}
SD & \text{ gives CD state (core disconnect), which is ideally high-Z} \\
SH & \text{ gives } V_H \\
SL & \text{ gives } V_L
\end{align*}
\]

With this provision, it may be possible (depending on the technology) to use either the \( V_H \) or the \( V_L \) state to provide for \( V_G \); this option is discussed in 8.2.2.

The remaining switches in the module could also be implemented as 3-state buffers, or, depending on the particular application and its sensitivity to switch resistance, they could be implemented as transmission gates.

7.3.3 Residual elements

7.3.3.1 Introduction

Many practical mixed-signal integrated circuits have one or more pins connected to circuit elements or networks that cannot be disconnected in test mode without severely compromising the...
component’s performance in mission mode. Examples are:

- A line driver may have an on-chip 50 \( \Omega \) termination resistor. To disconnect this would require a switch that could add unacceptable capacitance.

- High precision circuits may contain resistors connected directly to a pin for accuracy or matching reasons. A series switch could result in unacceptable mismatch or non-linearity.

In such cases, the core circuitry, which is isolated from the pin by the core disconnect switch, is considered to exclude these “residual elements”, which remain permanently connected to the pin. The term 'CD state' is used to indicate that the pin is effectively disconnected from the core but is not necessarily in the high-impedance state. Provided the residual elements are restricted in type and connectivity, the measurements made in test mode can be corrected to allow for their effects.

7.3.3.2 Specification of residual elements

Rules

(a) If any circuitry cannot be isolated from the function pins in test mode, it shall be capable of being modeled as a network of residual elements.

(b) Residual elements shall consist exclusively of linear passive components (resistors, capacitors, and inductors) together with independent dc voltage and current sources.

(c) If one end of a residual element is connected to an analog function pin, the other end shall be connected either to another analog function pin, or to a power supply pin, or to other residual elements.

NOTE - Reference supply pins are considered to be analog function pins.

(d) If one end of a residual element is connected to a digital function pin, the other end shall be connected to a power supply pin.

(e) Residual elements shall not connect to the core circuitry.

(f) All residual elements shall be documented.

NOTE - The documentation required for residual elements is detailed in Clause 10, which also specifies the way in which it must be presented.
Recommendation

(g) The use of residual elements should be avoided as far as possible without compromising mission function or performance.

Permission

(h) The residual element network may contain networks or devices whose model in terms of linear networks (as in 7.3.3.2(b) above) is valid only over a specified range of pin currents and voltages.

7.3.3.3 Description

Ideally, every pin, both input and output, would have the facility to be completely isolated from the internal circuitry while the component is in test mode: in other words, there would be core disconnect on every pin and there would be no residual components. The pins would then be driven by test signals applied through the ABM without either being influenced by signals from the core circuitry or injecting signals into the core circuitry. Allowing residual elements on output pins, and allowing input pins not to be equipped with core disconnect, are relaxations from the ideal that should be applied only when it is essential for operational reasons.

If residual elements are to be included in the component, it is important that their effects can be calculated so that measurements can be corrected and accuracy maintained. For this reason, residual elements must be documented (see 10.3), and they are restricted to linear networks: controlled sources are disallowed, since they are often particularly sensitive to measurement errors (small offsets can be multiplied and propagated through the system). It is, however, permitted for the residual “element” to take the form of a network rather than just a single element, provided that it can be modelled, over an appropriate range of current and voltage, as a network of linear passive elements and independent dc sources.

As well as restricting the types of permitted residual elements, the rules also restrict the connectivity.

Figure 22 illustrates some of the permitted and forbidden connections, with respect to a component with three analog pins, F1 - F3, one digital pin, F4, and a power supply pin, \( V_{SS} \). The CD switch between each analog pin and the core is shown, but the rest of the (standard) ABM is omitted for clarity. Each of the seven elements, E1 - E7, represents a passive element or an independent dc source.
E1, an element connected between two analog function pins, is allowed, as is E2, an element connected between an analog function pin and a power supply pin. E3, E4, and E5 represent a network of elements, each of which has one end connected to an analog function pin and the other end connected to another residual element. These elements are allowed. E6, connected between an analog function pin and a digital function pin, and E7, connected between a function pin and the core, are NOT allowed.

Figure 22: Connectivity of residual elements

7.3.4 ABM switch patterns

For the example ABM of Figure 19, all the rules will be satisfied if it is able to support the switch patterns specified in Table 6.
### Table 6: Switch patterns for example ABM of Figure 19

<table>
<thead>
<tr>
<th>Pattern</th>
<th>SD</th>
<th>SH</th>
<th>SL</th>
<th>SG</th>
<th>SB1</th>
<th>SB2</th>
<th>Pin state</th>
</tr>
</thead>
<tbody>
<tr>
<td>p0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>Completely isolated (CD state).</td>
</tr>
<tr>
<td>p1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>Monitored by AB2.</td>
</tr>
<tr>
<td>p2</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>Connected to AB1.</td>
</tr>
<tr>
<td>p3</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>Connected to AB1; monitored by AB2.</td>
</tr>
<tr>
<td>p4</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>Connected to $V_G$.</td>
</tr>
<tr>
<td>p5</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>Connected to $V_G$; monitored by AB2.</td>
</tr>
<tr>
<td>p6</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>Connected to $V_G$ and AB1.</td>
</tr>
<tr>
<td>p7</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>Connected to $V_G$ and AB1; monitored by AB2.</td>
</tr>
<tr>
<td>p8</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>Connected to $V_L$.</td>
</tr>
<tr>
<td>p9</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>Connected to $V_L$; monitored by AB2.</td>
</tr>
<tr>
<td>p10</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>Connected to $V_L$ and AB1.</td>
</tr>
<tr>
<td>p11</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>Connected to $V_L$ and AB1; monitored by AB2.</td>
</tr>
<tr>
<td>p12</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>Connected to $V_H$.</td>
</tr>
<tr>
<td>p13</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>Connected to $V_H$; monitored by AB2.</td>
</tr>
<tr>
<td>p14</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>Connected to $V_H$ and AB1.</td>
</tr>
<tr>
<td>p15</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>Connected to $V_H$ and AB1; monitored by AB2.</td>
</tr>
<tr>
<td>p16</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>Connected to core; isolated from all test circuits.</td>
</tr>
<tr>
<td>p17</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>Connected to core; monitored by AB2.</td>
</tr>
<tr>
<td>p18</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>Connected to core and AB1.</td>
</tr>
<tr>
<td>p19</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>Connected to core and AB1; monitored by AB2.</td>
</tr>
</tbody>
</table>

**NOTE 1** - In this table, each switch condition is denoted by 0 if the switch is open and 1 if the switch is closed, by reference to Figure 19. The logic signal that needs to be applied will be dependent on the particular implementation.

**NOTE 2** - If additional optional analog test lines are provided, SB1 would be connected to one of the input bus lines (AB1 or AB1N) and SB2 would be connected to one of the output bus lines (AB2 or AB2N).
The reasons for requiring these switching patterns are summarized in Table 7.

### Table 7: Functions of ABM switching patterns

<table>
<thead>
<tr>
<th>Patterns</th>
<th>Comments</th>
</tr>
</thead>
<tbody>
<tr>
<td>p0</td>
<td>Pin isolated both from the core and from all the test circuitry.</td>
</tr>
<tr>
<td>p1 - p5</td>
<td>These are the main testing conditions for analog measurements, the function pin is isolated from the core, but is connected to one or both internal bus lines. It is used for extended interconnect measurements.</td>
</tr>
<tr>
<td>p6 - p7</td>
<td>These can be used to test the parametric behavior of the reference quality voltage.</td>
</tr>
<tr>
<td>p0, p8, p12</td>
<td>Logic values (or CD state) for simple interconnect testing.</td>
</tr>
<tr>
<td>p9 - p11, p13 - p15</td>
<td>Combination of logic values and analog buses allows (e.g.) parametric measurements of $V_H$ and $V_L$ sources, or biasing external components while making analog measurements.</td>
</tr>
<tr>
<td>p16</td>
<td>Normal mission mode: pin connected to core only.</td>
</tr>
<tr>
<td>p17 - p19</td>
<td>Testing conditions used in PROBE and INTEST.</td>
</tr>
</tbody>
</table>

Additional connection patterns could be provided to support optional user-defined instructions; additional switches may also be fitted to increase flexibility, but the consequential effects on parasitic loading of the test buses will need to be taken into account.

These patterns will be invoked as appropriate to serve the needs of the various instructions as shown in Table 8, which shows a set of patterns that supports all defined instructions.
Table 8: ABM switching pattern requirements

<table>
<thead>
<tr>
<th>Code C/D/B1/B2 (see Figure 23)</th>
<th>Instruction</th>
<th>Code C/D/B1/B2 (see Figure 23)</th>
<th>Instruction</th>
</tr>
</thead>
<tbody>
<tr>
<td>0000</td>
<td>p0</td>
<td>1000</td>
<td>p8</td>
</tr>
<tr>
<td>0001</td>
<td>p1</td>
<td>1001</td>
<td>p9</td>
</tr>
<tr>
<td>0010</td>
<td>p2</td>
<td>1010</td>
<td>p10</td>
</tr>
<tr>
<td>0011</td>
<td>p3</td>
<td>1011</td>
<td>p11</td>
</tr>
<tr>
<td>0100</td>
<td>p4</td>
<td>1100</td>
<td>p12</td>
</tr>
<tr>
<td>0101</td>
<td>p5</td>
<td>1101</td>
<td>p13</td>
</tr>
<tr>
<td>0110</td>
<td>p6</td>
<td>1110</td>
<td>p14</td>
</tr>
<tr>
<td>0111</td>
<td>p7</td>
<td>1111</td>
<td>p15</td>
</tr>
</tbody>
</table>

Clause 1- *RUNBIST* will select the same switching patterns as *CLAMP* if the option in 5.4.3.1(b)(i) is exercised.

Clause 2- *RUNBIST* will select the same switching patterns as *HIGHZ* if the option in 5.4.3.1(b)(ii) is exercised.

Clause 3- *HIGHZ* requires p0 for all codes.

Clause 4 - All other defined instructions (*BYPASS, SAMPLE/PRELOAD, IDCODE, and USERCODE*) require p16 for all codes.

Clause 5 - Code bits are CONTROL (C), DATA (D), BUS1 (B1) and BUS2 (B2); instructions are represented by mode bits supplied by the instruction decoder.

Clause 6 - Entries marked with an asterisk are undefined. The effects produced by the corresponding codes would depend on the particular implementation. In general, it would not be good practice to allow such codes to be entered by the test program, since they could be assigned specific functions in future revisions of the standard.

Clause 7 - The assignments of switching patterns to codes for user-defined instructions is not restricted. Such assignments would be selected when the appropriate user-defined instruction code is decoded by the instruction decoder.
7.3.5 Control of the ABM

7.3.5.1 Specification

Rules

(a) Each ABM shall contain a control register and an update register.

(b) The control register shall consist of four stages, identified by the labels BUS1, BUS2, CONTROL, and DATA.

(c) The control register shall form part of the boundary-scan register.

(d) The update register shall be parallel loaded from the control register and any necessary combinational logic in response to the falling edge of TCK while the TAP controller is in the Update-DR state.

(e) The control circuitry of the ABM shall be designed so that the contents of the update register together with signals derived from the TAP controller and the instruction decoder allow operation in accordance with the operating modes specified in 7.3.4, Table 6 and Table 8.

(f) The result of the digitization of the pin voltage shall be captured in the DATA stage of the control register on the rising edge of TCK while the TAP controller is in the Capture-DR state.

Permissions

(g) Other stages of the ABM control register may be used at the designer's discretion to capture internal states on a rising edge of TCK while the TAP controller is in the Capture-DR state, provided that no rules of this standard are violated.

NOTE - Values captured into the control register could be transferred into the update register with unforeseen consequences if particular sequences of TAP controller states are executed (e.g., CAPTURE-DR, EXIT1-DR, UPDATE-DR).

(h) When the control register stages are incorporated into the boundary-scan register, they may be grouped and ordered in any way to suit the convenience of the manufacturer.
7.3.5.2 Description

A possible implementation of an ABM that satisfies all of the rules in this standard is shown in Figure 23, in which the control register consists of the four flip-flops at the bottom of the diagram, the other four flip-flops forming the update register.

![Figure 23: Possible control structure for ABM](image)

The control signals for the individual switches are derived by the control logic from the contents of the Update register together with a set of Mode signals (Mode1 and Mode2) which would be supplied by the instruction decoder. The number of Mode signals needed will depend on the range of instructions to be supported.

The control logic in Figure 23 could satisfy the switching pattern requirements of Table 8 if it implements the following equations, where the control signal needed to activate each switch is given the name of the switch.
[CONTROL = C; DATA = D; BUS1 = B_1; BUS2 = B_2; Mode1 = M_1; Mode2 = M_2.]

\[
\begin{align*}
SD &= \overline{M}_1 \\
SH &= CD M_1 M_2 \\
SL &= \overline{C}D M_1 M_2 \\
SG &= \overline{C}D M_1 M_2 \\
SB_1 &= B_1 M_2 \\
SB_2 &= B_2 M_2 
\end{align*}
\]

In the circuit of Figure 23, the mode signals used (M_1 and M_2) are those defined in Table 9, and are sufficient to support all the mandatory and optional instructions defined in IEEE Std 1149.1 and this standard.

Table 9 : Required mode signals for example ABM (Figure 23)

<table>
<thead>
<tr>
<th>Instruction</th>
<th>Mode1</th>
<th>Mode2</th>
</tr>
</thead>
<tbody>
<tr>
<td>EXTEST, CLAMP, RUNBIST</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>PROBE, INTEST</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>HIGHZ</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>Other instructions</td>
<td>0</td>
<td>0</td>
</tr>
</tbody>
</table>

NOTE - “Other instructions” include BYPASS, SAMPLE/PRELOAD, IDCODE, and USERCODE.

The other control signals used in the circuit of Figure 23 are UpdateDR, ShiftDR, and ClockDR, which would be generated by the TAP controller (as in the example TAP controller implementation shown in IEEE Std 1149.1). These signals are used to control the entry into the ABM registers of data supplied serially through TDI, the capture of digitized data, the transfer of data to the update register, and the serial inspection of data through TDO.

The control register is loaded with data in one of two ways:

(i) on the rising edge of TCK while the TAP controller is in the Shift-DR state : this allows the register to be loaded serially with internal data from TDI;
(ii) on the rising edge of TCK while the TAP controller is in the *Capture-DR* state: this allows the register to be loaded in parallel with external data, which can subsequently be shifted out serially through TDO.

When it comes to the physical layout of a component, because the individual stages of the control register are identified by name, the ordering of the stages within the boundary-scan register is at the discretion of the designer, and they do not even need to be kept as a single group.

If access to other internal nodes for test purposes is not required, the additional capture points, and their associated multiplexers, need not be provided. However, they do provide an opportunity to access other internal nodes in the component, and for the cost of a multiplexer it may well be seen as a worthwhile testability enhancement. Good candidates for capture, for example, would be the BUS1 and BUS2 update register stage outputs, which are not otherwise accessible.

### 7.4 Differential analog boundary modules

#### 7.4.1 Specification

Rules

(a) An ABM shall be connected to each analog differential pin.

(b) The ABM connected to a differential pin shall provide the same facilities, and obey the same rules, as an ABM connected to a single-ended analog pin.

NOTE 1 - This implies that each ABM has a control register and an update register, and that the switch patterns in Table 6 are applicable.

NOTE 2 - The two control registers are both part of the boundary-scan register, and the individual stages are identified in each case as BUS1, BUS2, CONTROL, and DATA.

NOTE 3 - Codes are entered independently into the two control registers, as in Table 8, to identify required switch patterns.

(c) The ABMs connected to a pair of differential output pins shall be controlled jointly such that

(i) Either, neither, or both pins can be isolated from the core and from all dc test signals (i.e., with SD, SG, SH, and SL switches all open).
(ii) Either pin can be connected to $V_G$ (i.e., with SG closed and SD, SH, and SL open) while the other pin is isolated from the core (i.e., with SG, SD, SH, and SL all open).

(iii) Either pin can be connected to $V_H$ (i.e., with SH closed and SD, SG, and SL open) while the other pin is connected to $V_L$ (i.e., with SL closed and SD, SH, and SG open).

(d) The ABMs connected to a pair of differential input pins where a core disconnect facility is implemented shall be controlled jointly as in (c) above.

(e) The ABMs connected to a pair of differential input pins where a core disconnect facility is not implemented shall be controlled jointly such that

(i) Either pin can be connected to $V_G$ (i.e., with SG closed and SH and SL open) while the other pin is isolated from all dc test signals (i.e., with SG, SH, and SL open).

(ii) Either pin can be connected to $V_H$ (i.e., with SH closed and SG and SL open) while the other pin is connected to $V_L$ (i.e., with SL closed and SH and SG open).

(f) In all of the conditions (c) to (e) above, it shall be possible also to connect either pin to either or both of AB1 and AB2 (i.e., with SB1 and/or SB2 closed).

   NOTE: If the optional buses AB1N or AB2N exist, then the inverting pin shall connect to AB1N and AB2N instead of AB1 and AB2.

(g) If the codes entered into the two ABMs correspond to a pair of pin-states other than those defined in (c) to (f) above, the states assumed by the pins shall be at the discretion of the manufacturer.

(h) The BUS1 bit in the ABM control register attached to the non-inverting input of a differential receiver shall capture either the digitized voltage difference between the pins, or (if it would give the same result) the output of the differential receiver.

(i) The BUS1 bit in the ABM control register attached to the non-inverting output of a differential driver shall capture the digitized voltage difference between the pins.

(j) If INTEST or RUNBIST is supported, a control and observe DBM shall be connected between each differential receiver/driver and the core circuitry.
Recommendation

(k) The undefined states in (g) above should be defined and documented.

Permission

(l) ABMs may be connected to digital differential pins as long as they follow the rules above.

7.4.2 Description

A differential ABM consists essentially of two single-ended ABMs, with added differential observation capabilities. The difference lies in the control: a differential ABM is permitted to produce a subset of all combinations of drive states that would be available from a pair of independent single-ended ABMs. This allows the testing of common differential circuits with less impact on their normal performance.

A differential driver will often be incapable of driving all possible pairs of states onto the two pins: for example, the output might be forbidden by circuit topology from driving both pins simultaneously to logic 1 or both simultaneously to logic 0. While it might be possible to add additional circuitry to force all possible state pairs for test purposes, this might degrade normal circuit performance to the extent that the benefits of differential drive are lost.

Table 10: Switch pattern combinations for differential pins

<table>
<thead>
<tr>
<th>Inverting driver switch pattern (see Table 6)</th>
<th>Non-inverting driver switch pattern</th>
</tr>
</thead>
<tbody>
<tr>
<td>CD (p0 - p3)</td>
<td>CD</td>
</tr>
<tr>
<td>G (p4 - p7)</td>
<td>R</td>
</tr>
<tr>
<td>L (p8 - p11)</td>
<td>×</td>
</tr>
<tr>
<td>H (p12 - p15)</td>
<td>×</td>
</tr>
</tbody>
</table>

Therefore, this standard requires a differential driver to produce as few as 5 state pairs: H-L, L-H, CD-CD, CD-G, and G-CD. This is summarized in Table 10, which indicates with R the state-pairs that are required by the rules to be available, and also shows that, if other state-pairs are selected by the codes in the ABMs, the outcome (indicated by ×) is at the discretion of the manufacturer (i.e.,
in general, it is unpredictable; the manufacturer is recommended, but not obliged, to document it). It is up to the user to avoid using these “don’t care” code combinations in the test program, while it is prudent for the manufacturer to use caution in design, to avoid damage to the component or its surroundings if these states are asserted accidentally.

If the pins have residual elements connected to voltage or current supplies adequate for carrying test currents, then it may be possible to subsume the G state into the CD state. If the H or L state produces a reference quality output voltage, that state may be the same as the CD state, reducing each driver pin to a two-state driver.

Figure 24 shows a differential input using a differential ABM. The differential ABM merges two single-ended ABMs, each with a four bit update register and up to four bits of capture, while retaining all essential capabilities of two separate ABMs. Each side of the differential ABM illustrated may independently connect AB1 or AB2 to each pin, and drive each pin with $V_G$, $V_H$, or $V_L$. Each of the two ABMs captures a single-ended value using a digitizing receiver and stores the result in the DATA
bit of the capture (control) register. The thresholds of these digitizing receivers will typically be related to the common mode voltage of the differential signal, which might not be defined well enough for reliable single-ended capture. To ensure a valid logic state is always captured, the differential signal is also compared with a zero-offset differential digitizing receiver or comparator, to be captured by the BUS1 bit of the non-inverting control register. This digitizing receiver may be merged by the designer with the normal input receiver if that receiver is made without significant offset or hysteresis.

If a digital input differential receiver contains ABMs and connects to a core which has INTEST capability, the digital values created at the ‘analog’ to digital boundary (as defined in IEEE Std 1149.1) must be routed through DBMs. This allows a digital INTEST to proceed in a defined way, regardless of the state of the pin.

![Figure 25: A differential output using a differential analog boundary module](image)

Though not shown in Figure 24, the AB1 and AB2 connections on the inverting pin of the differential ABM may instead be connected to the optional internal differential lines AB1N and AB2N for a full differential measurement. As discussed later in this clause, this is also possible for output and bi-directional versions of the differential ABM, for both digital and analog pins.
Figure 25 shows a differential output using a differential ABM. Signals to control the output driver transistors, or to route normal signals to the transistors during mission mode, are derived from the update/control registers by appropriate decode logic. Like the differential input ABM, the single-ended output pin values are captured by digitizing receivers to drive the DATA bit of the control register for each pin. Also like the differential input, the difference between the pins is captured by the BUS1 bit of the non-inverting pin’s control register. The BUS1 and BUS2 update bits control switches from the pins to AB1 and AB2, with optional connections to AB1N and AB2N from the inverting pin’s switches. If INTEST is implemented, and this differential output is used for digital signals from the core, then a digital boundary module is required at the input to the driver.

Figure 26 shows an example of a differential output driver with resistive loads. The N channel FET differential pair switches current between the left and right load resistors, which are included in the residual elements and are not core disconnectable. Since there is only one source of current, only one resistor may be pulled down and therefore only one pin may be driven to $V_L$. However, both FETs may be turned off, and both pins are pulled high to the $V_{DD}$ supply. If the $V_{DD}$ supply is reference quality, the resulting H-H state may be used as both the CD-CD state and as the CD-G and G-CD states, since the resistors provide a current return for parametric test. However, the resistors may have such a large variance that they make accurate measurement of external resistors difficult; if
external resistors require accurate measurement, the internal resistors must be completely disconnected in the CD state.

If the differential driver is not capable of producing reference quality output voltages (because the driver has a large offset voltage or its power supplies are not reference quality), then separate SG switches to a $V_G$ will be required, and the conductive paths through the normal driver networks must be switched off.

Parametric measurement accuracy will be maximized when the impedance of each pin is relatively high when the core is disconnected and relatively low when the SG switches are enabled. Simple interconnect test is most effective when the SH and SL switches are capable of driving each of the pins in the differential pair independently and with a large voltage swing, thus allowing the driver to produce the same voltage excursions that a pair of independent ABMs is capable of producing.

### 7.4.3 Differential testing

Fully differential testing requires an extension to the ATAP, to accommodate a differential pair of input pins (AT1 and AT1N) and a differential pair of output pins (AT2 and AT2N). The additional external test bus lines will also need to be matched with two corresponding internal analog bus lines (AB1N and AB2N). There will be a second TBIC attached to AT1N and AT2N, as shown in Figure 27. The fact that the two pins of a differential pair have a functional relationship means that each ABM needs to have access to only two of the four analog test bus lines: as shown in Figure 27, the non-inverting pins would access AB1 and AB2, while the inverting pins would instead access AB1N and AB2N. To facilitate optimal differential performance, path impedances should be matched within each bus pair (AB1 and AB1N, and AB2 and AB2N).

![Figure 27: Differential testing of core](image-url)
If AB1N and AB2N are not implemented, it is possible to test differential circuitry in stages, as illustrated in Figure 28. This shows AB1 connected to the non-inverting input while the inverting input is held at $V_G$ (or $V_H$ or $V_L$). The inverting and non-inverting outputs can then be observed in turn through AB2. The process can then be repeated, stimulating the inverting input and observing the two outputs in turn. This would, in many cases, provide effective functional testing without incurring the cost of the extended ATAP.

Figure 28: Testing a differential circuit without differential facilities
8 Measurement Methodology

8.1 Interconnect testing

8.1.1 Simple interconnect testing

The *EXTEST* instruction allows the testing of simple interconnect (i.e., testing for open circuits in the direct net connection between components, and bridges between nets) for the ATAP pins as well as all function pins (both analog and digital), by loading digital test data into output modules and capturing responses at input modules. In the case of digital pins, the test data is loaded directly into the DBMs; in the case of analog pins, the data loaded into the ABMs consists of control codes that cause internally generated values (\(V_H\) or \(V_L\)) to be applied to the pin when the *EXTEST* instruction is selected. The voltage values used for \(V_H\) and \(V_L\) while the *EXTEST* instruction is selected are those used to represent logic 1 and logic 0, and for analog pins these values are the maximum and minimum values attainable in normal functional use.

The test begins with data for the first test being shifted into the output modules in the boundary-scan register (typically using the *PRELOAD* phase of the *SAMPLE/PRELOAD* instruction) and applied to the external interconnect when the *EXTEST* instruction is selected in the *Update-IR* controller state. The results of the test are captured in the input modules of the boundary-scan register in the *Capture-DR* controller state, and shifted out in the *Shift-DR* controller state at the same time that data for the next test is being shifted in. This sequence of operations is identical to that used in IEEE Std 1149.1.

The *EXTEST* instruction can also be used to check for open-circuit and bridging faults within extended interconnect (see Figure 2). In this case, all analog pins that are connected to discrete components are to be treated as output pins (i.e., they will all be supplied with test data). Test results in this case are obtained by monitoring the voltage actually appearing at the pin, and capturing a binary equivalent of this voltage back into the original driving module. Rule 7.3.1(f) ensures that the necessary capability is provided in the ABM.

8.1.2 Differential interconnect testing

The approach to be taken in dealing with interconnections between differential input/output pins and the circuits attached to them will depend on the facilities that are provided within individual components.

Within the terms of this standard, it is not mandatory to provide differential test facilities (i.e., ATAP
pins AT1N and AT2N and internal test buses AB1N and AB2N), even if some of the inputs or outputs are differential. However, every analog function pin, whether input or output, single-ended or differential, must be equipped with an ABM. It will, therefore, be possible, as shown in Figure 29, to apply logic signals to, and collect logic responses from, each individual analog differential interconnect line; the core disconnect facility ensures that the internal circuitry is not damaged by driving the differential pins non-differentially.

One way of dealing with digital differential pins is to regard all such pins as analog (which is the approach adopted in IEEE Std 1149.1). Adopting this approach within the context of this standard would mean that all differential pins, input and output, would be fitted with ABMs as shown in Figure 29. This would allow not only the application of logic signals for simple interconnect testing, but also the use of AT1 and AT2 to perform analog measurements on the discrete circuitry connected between the chips (see 8.2 and 8.3). If the performance impact of inserting an ABM into the input circuitry is unacceptable, simple interconnect testing on digital differential interconnect could be facilitated by

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equipping the outputs with full DBMs and the inputs with observe-only DBMs as illustrated in Figure 30.

Provided that all the pins are equipped with boundary modules of one kind or another, testing of simple interconnect on both analog and digital differential lines can be achieved at the same time with EXTEST, with data being applied and collected through the boundary-scan register, using the same procedures as outlined in 8.1.1.

All required differential outputs should be provided by the normal system driver, just as in the single-ended case. Some of the conceptual switches can be built into the differential output driver; such a driver has to be capable of driving either or both outputs to CD state.

8.1.3 Differential I/O

Differential I/O is often used, as shown in Figure 3, to convey a single-ended output signal to a single-ended input signal, where the transmission channel is expected to experience significant common-mode noise. In such a case, there would be benefits in being able to test the transmission from the single-ended output to the single-ended input.

![Figure 31: Provision for testing differential communication between chips](image)

This test requires control and observation of the single-ended signals by including internal test modules at these points as shown in Figure 31. If these are analog modules, they could be similar to ABMs, but simplified since the switches provided in the normal ABM for testing simple interconnect between pins would not be required. These internal modules would not be included in the boundary-scan register, and they would need to be accessed by a user-defined instruction that would leave the
boundary-scan ABMs in normal mission mode (i.e., with the core disconnect switch closed and the pin disconnected from all test circuitry).

An alternative approach for a differential input is to insert an optional boundary-scan cell, as described in IEEE Std 1149.1, to sample the difference between the two differential signals, e.g., to sample the output of a comparator whose two inputs are appropriately connected to the two pins' signals.

### 8.2 Extended interconnect testing

#### 8.2.1 Virtual probing

Traditional in-circuit test involves connecting the probes of an in-circuit tester to a component on a board (the CUT) in such a way as to place it in the feedback path of an operational amplifier, forcing a known current through the CUT, and measuring the resulting voltage across the CUT.

![Figure 32: Principle of analog component measurement](image)

This simple picture is modified in conventional in-circuit test, because the CUT is embedded in a circuit on the printed circuit board. To preserve accuracy in measurement, grounded "guarding" probes have to be used to force the test current to flow only through the CUT, making use of the virtual ground property of the operational amplifier.
With the structure used in this standard, the classical in-circuit measurement technique has to be modified. Although the switches SB1 and SB2 in the ABM permit the analog bus lines to be connected to any component pin on the board, and so are analogous to the probes of an in-circuit tester, there is an important difference: the switches will, in most practical cases, have an on-resistance which is significant compared with the impedance of the CUT (see Figure 51).

The principle of making an analog measurement without using guarding and without requiring any zero-ohm connections between the ATE and the CUT is illustrated in Figure 32 for the case of an impedance connected between a component pin and ground. An ac test current, $I_T$, is applied through AT1 which is in turn connected to the component pin by way of switches S5 (in the TBIC) and SB1 (in the ABM). The applied current can be measured in the ATE, and a complex voltage measurement (amplitude and phase) made at AT2, which is connected to the component pin through switches S6 (in the TBIC) and SB2 (in the ABM). The measured voltage, $V_T$, will be a good approximation to the voltage across the CUT if

$$Z_V \gg Z_{S6} + Z_{SB2},$$

and the current, $I_T$, will be a good approximation to the current through the CUT if

$$Z_V + Z_{S6} + Z_{SB2} \gg Z_D$$

where

- $Z_V$ is the impedance of the voltage measurement system,
- $Z_{S6}$ is the impedance of switch S6,
- $Z_{SB2}$ is the impedance of switch SB2,
- $Z_D$ is the impedance of the CUT.

These conditions will normally be satisfied if the voltage measurement is made using a high impedance measurement system.

Finally, the impedance of the CUT is given by $Z_D = V_T / I_T$.

**8.2.2 Extended interconnect measurements**

The simplest form of extended interconnect consists of a simple series component connected between two component pins, F1 and F2, which could be on the same component. The principle of the measurement technique is to pass a known current through the CUT, and calculate the voltage across it by measuring the voltage appearing at each end.

There are altogether at least five pins involved in the measurement process at any one time. The simplest setup is shown in Figure 33, in which a circuit under test (CUT) is connected to two function pins F1 and F2.
Figure 33: Measuring CUT connected between function pins - first measurement

[TBIC and ABM switches shown are closed; all others are open]

The other pins actively involved in the measurement are AT1, AT2, and $V_G$, and in Figure 33 these pins are shown connected (via the TBIC and ABM switches) to F1, F1, and F2 respectively. Note that the node marked “common node” is inside the tester. If $V_G$ is GND, this is the simplest setup, and if the chip is supplied with a GND pin, then this is what would normally be used for $V_G$. For the first measurement, illustrated in Figure 33, a current stimulus, $I_T$, is applied by the ATE through AT1 to F1, while F2 is connected to $V_G$.

If there is no GND pin, we have the situation shown in Figure 34, where the $V_G$ pin is an existing pin of the chip which is driven externally from a near-ideal voltage source. In all probability, this would be one of the power supply pins of the chip ($V_{DD}$, $V_{SS}$, etc), but if the chip has a reference supply pin this can be used for $V_G$ provided the $V_G$ supply can deliver (source/sink) the required range of current while still acting as an ideal voltage source.

In this case, with $V_G$ being a non-zero supply, there is also a further option. We can connect the common node directly to the $V_G$ pin (marked P in Figure 34), or we could connect it to the tester GND (Q in Figure 34). The choice would be a matter of convenience for the tester.

Notice that the requirement placed on the reference quality voltage source is that it must sink the current $I_T$ without suffering any appreciable change in the value of $V_G$ (i.e., it must be a good voltage source). It is also clear that $V_G$ must be available at a pin, since that is the only way that a common reference can be established between $V_G$ and the measuring equipment.
The configurations in Figure 33 or Figure 34 can always be used, but they require the use of physical switches to apply $V_G$ to the function pin. With some technologies, it may be possible to provide a more economical solution, as illustrated in Figure 35.

Here pin F2 is connected to an output driver, one of whose power supplies is $V_G$. The driver is built in such a way that internal logic signals (labelled SH and SL) can be applied to produce $V_H$ or $V_L$ at the output, as indicated in Figure 21. If the application of SL to the driver produces at the function pin a voltage that is very close to $V_G$ and, over a specified range of test currents, very nearly
independent of the current flowing through the pin, then the setup shown in Figure 35 can be used. Again, if the value of $V_G$ is not zero, the common node can be connected to either side of the voltage source as in Figure 34.

![Figure 36: Measuring CUT connected between function pins - second measurement](image)

The experimental setup for making the second voltage measurement on the CUT is essentially the same, except that the measurement, $V_{F2}$, is obtained by connecting F2 to AT2 through switches SB2 and S6 as shown in Figure 36. The same considerations with regard to the reference node apply again: Figure 36 assumes that $V_G$ is GND. Nearly all the current through the CUT will pass through switch SG to the reference source $V_G$ provided that

$$Z_V + Z_{S6} + Z_{SB2} \gg Z_{SG}$$

If this is satisfied, $V_{F2}$ will then be a good approximation to the voltage at F2 in Figure 33 if

$$Z_V \approx Z_{S6} + Z_{SB2}$$

so that the impedance of the CUT can be calculated as

$$Z_D = \frac{V_{F1} - V_{F2}}{I_T}$$
Apart from the inequalities noted above, which will normally be easily satisfied since the voltage measuring device attached to AT2 will have an impedance much larger than that of the CUT and the switches, the accuracy of the results will be affected by two other considerations.

(i) The stability of the reference supply \( (V_G \text{ in Figure 33 and Figure 36}) \) over the time taken to make the pair of measurements;

(ii) The resistance between the point at which the two switched paths join and the point of entry to the CUT must be negligible (see 9.3 and Figure 39: this resistance is \( R_{\text{com}} \)).

### 8.3 Network measurements

The measurement of more general networks connected between components can be approached in a similar manner. Figure 37, for example, shows a typical two-port network, which could be a passive filter or an attenuator, connected between pins P1 and P2 on one component, and P3 and P4 on another. All the pins are assumed to be equipped with ABMs, which means that any number of experiments can be set up in which the ATE applies a known test current to one of the pins (e.g., P1 in Figure 37) and measures the voltage at the same or a different pin (e.g., P3 in Figure 37), while any of the pins involved can be left open circuit or connected to a reference voltage (e.g., P4 is connected to \( V_G \) in Figure 37). The connections are made through AT1 and AT2 using the methods described in 8.2.

![Figure 37: More Complex Interconnect Network](image)

Keeping the configuration undisturbed, the ATE can measure the voltage at each pin in turn, and assuming as before that the loading effect of the voltage measuring system can be disregarded, these measurements permit the branch voltages to be calculated - e.g., the voltage across \( Z_1 \) is given by

\[
V_{12} = V_{P1} - V_{P2}.
\]

Two experiments can be performed: the first (illustrated in Figure 37) with a current \( I_{T1} \) applied to
P1 with P3 open circuit and P2 (or P4) connected to a reference \( (V_G) \); and the second with current \( I_{T2} \) (where \( I_{T2} \) could be, but is not necessarily, the same as \( I_{T1} \)) applied to P3 with P1 open circuit.

With this particular network, there are five unknowns: the three impedances \( Z_1, Z_2, \) and \( Z_3 \), the applied reference voltage, \( V_G \), and the switch impedance associated with \( V_G \). With three voltage measurements obtained from each of the two experiments, we therefore have enough data with which to calculate the three branch impedances of interest. For more complicated networks, where the number of elements exceeds the number of measurements that are available, a special metrology has been developed using simulation to supply additional data. This metrology is fully described in the paper by Parker et al (see 1.4).
9 Analog parametric limits

9.1 General

An objective of this standard is to facilitate measurement of complex impedances with an accuracy better than ±1% when measuring impedances between 10 Ω and 100 kΩ, with a 1 kHz bandwidth anywhere between 100 Hz and 10 kHz. Many systematic sources of error can be characterized and hence may not contribute to this error. Other sources cannot be measured and must be minimized. The ability to achieve this level of accuracy ultimately depends upon the analog characteristics of the buses, the switches, the CUT, and the ATE. These in turn depend on the way the standard is implemented, and also on details of the layout and design. This clause defines performance limits that need to be met if the required accuracy is to be achieved, based on measurements that can be made using the test bus structure itself.

Factors that affect performance include the way in which the switches in the TBIC and the ABMs are implemented, and also the measures taken to provide electrostatic protection to the chip. The rules that follow try to anticipate a large variety of power supply voltages, switch implementations, and bus architectures, while assuming use of state-of-the-art measurement equipment and techniques.

The standard provides facilities for calibration, which allows some potential errors to be cancelled or compensated, but there will be other errors due to inevitable practical limitations; these will have to be minimized by careful design.

In the remainder of this clause, the most positive and negative pin-specific power supply voltages are denoted by $V_{DD}$ and $V_{SS}$ respectively. Some voltages and resistances are only measurable in certain ABM and/or TBIC states, and may not correspond to a specific pin or element. For example, $V_{ip}$ is the unloaded voltage present at a function pin, and might be equal to the voltage ($V_{DD}$) at the $V_{DD}$ pin minus some offset voltage; $R_{sw1}$ is the resistance across two switches ($S6$ and SB1) and is measurable only as the sum of the switch resistances, $R_{S6} + R_{SB1}$.

9.2 Switch limitations

The key architectural features of this standard are the TBIC and the ABM, both of which are defined as consisting largely of conceptual switches. When the standard is implemented, these conceptual switches can be realized in a number of ways. It might be convenient, for example, particularly in CMOS circuits, to use transmission gates; in some cases the necessary switching functions can be integrated with system drivers or receivers; and any or all of the switches may be implemented using 3-state voltage buffers and/or current buffers, as shown in Figure 38.
Figure 38: Switches implemented as buffers

When transmission gate switches are used, the impedance of the path between AT1 and a function pin is likely to be significant compared with the impedance of the CUT. However, the metrology of this standard does not depend on a specific or low resistance for the AB1 and AB2 switches: as long as the resistance is constant, it can have any unknown value, within limits that are orders of magnitude apart. The upper bound on switch path resistance is required only to ensure that test current can be passed through the path without the need for excessive voltages to be applied. A lower bound is required so that test voltages can be applied without excessive current flowing.

The maximum output impedance of a function pin, when only its SG, SH, or SL switch is closed, should be as small as practicable, since a low value for the SG switch resistance reduces measurement error, and low values for the SH and SL switch resistances allow fast interconnect testing.

When 3-state voltage buffers and/or current buffers are used to implement the switches, as shown in Figure 38, their gain does not need to be unity. In all cases, the gains and impedances in the AT1/AB1 and AT2/AB2 paths can be characterized to allow accurate measurements of circuits under test.
9.3 Electrostatic protection

9.3.1 Specification

Recommendation

(a) Any series impedance irremovably connected in a path that is common to the connections between the function pin and the two internal bus lines (i.e., $R_{com}$) should have an impedance of less than 1 Ω.

NOTE - This impedance must be documented.

9.3.2 Description

It is typical, especially for CMOS integrated circuits, to incorporate ESD protection circuitry near or in the pad input receiver or output driver. Often, when designing an integrated circuit, a relatively large resistance is placed between a bonding pad and its associated input buffer; the input buffer's capacitance is very small and even 1 kΩ typically adds less than 100 ps delay. For an output driver, only a much smaller resistance is tolerable between the pad and the buffer, so as to minimize the effect on the output impedance or delay (when driving large off-chip capacitances). These ESD protection resistances will appear in series with any off-chip impedance connected to the function pin being tested via AB1 and AB2. If these resistances (shown as $R_5$ in Figure 39) are included in the value of the impedance measured via these buses, this could represent a significant error.

By appropriately connecting the ABM switches to the analog function pin's bonding pad, the value of any series ESD-protection resistances can be cancelled: this is equivalent to the Kelvin four probe measurement technique. The technique sources measurement current from one probe, sinks the current through a second probe, and monitors voltage across the resistance of interest using two additional probes. This implies that ESD protection resistance(s) used for signals that drive a pad (including the output function driver, the SB1 switch, the SG switch, and the SH and SL switches) should be separate from those used for signals received from the pad (including the input function receiver, the SB2 switch, and the $V_{TH}$ comparator), as shown in Figure 39(a).

In practice, it is difficult to avoid having some common resistance, $R_{com}$, between the internal bus lines and the CUT, as shown in Figure 39(b). Any such common resistance, due to ESD protection resistance, the bond wire, and/or the package pin, will unavoidably be measured in series with the CUT. The resistance should be as close to zero as possible, considering the values of off-chip impedance likely to be measured, but, in any case, its value will have to be documented because it affects all measurements.
9.4 Performance specifications

Rules

(a) When transmission gate switches are used, $R_{sw1}$, the maximum incremental switch resistance in the AT1 path (measured between AT1 and each function pin while the function pin is driven to any dc voltage between $V_{DD}$ and $V_{SS}$), shall be

\[
\frac{V_{DD} - V_{SS} - 200 \text{ mV}}{200 \mu \text{A}} \quad \text{or} \quad 10 \text{ k}\Omega
\]

NOTE - This will include the TBIC AT1-AB1 switch (S5 in Figure 12 and Figure 42).

(b) When transmission gate switches are used, $R_{sw2}$, the maximum incremental switch resistance in the AT2 path (measured between AT2 and each function pin while the function pin is driven to any dc voltage between $V_{DD}$ and $V_{SS}$), shall be 10 k\Omega.

NOTE - This will include the TBIC AB2-AT2 switch (S6 in Figure 12 and Figure 43).

(c) When the function output driver for an output pin is not used for driving $V_H$ and $V_L$, the
maximum output resistance for $V_H$ and $V_L$, measured between the function pin and $V_{DD}$ or $V_{SS}$ respectively shall be 10 k$\Omega$.

NOTE - This will include the ABM switch between the function pin and $V_H$ or $V_L$ (SH or SL in Figure 19).

(d) The maximum output resistance for $V_G$, measured between each function pin and the pin used to supply (see 10.2.1), using a 100 µA amplitude, 1 kHz sine wave stimulus current, shall be $\frac{V_{DD} - V_{SS} - 200 \text{ mV}}{200 \mu\text{A}}$ or 10 k$\Omega$, whichever is less.

(e) When a current buffer is used as a switch in the AT1 to AB1 path, or in the AB1 to function pin path,

(i) it shall be capable of delivering a 1kHz sine wave stimulus of 100 µA peak amplitude at the function pin;

(ii) the absolute value of the current gain shall be between 0.5 and 2;

(iii) input currents that exceed the capability of the buffer shall cause the buffer to saturate.

NOTE - Since the current gain is not necessarily unity, the current range at AT1 may be less than ±100 µA.

(f) When a voltage buffer is used as a switch in the function pin to AB2 path, or in the AB2 to AT2 path,

(i) it shall be capable of monitoring a 1 kHz sine wave stimulus of 100 mV peak amplitude with a bias of any voltage between $V_{DD}$ and $V_{SS}$ at the function pin;

(ii) the maximum absolute value of the voltage gain shall be unity;

(iii) input voltages that exceed the capability of the buffer shall cause the buffer to saturate.

NOTE - Because the voltage gain may be less than unity, the voltage range at AT2 may be less than its $V_{DD} - V_{SS}$.

(g) When delivering, via AT1, a 1 kHz sinusoidal current of 100 µA amplitude to a 1 k$\Omega$ resistor connected to a function pin, and measuring the voltage via AT2 using a voltmeter
with a -3 dB bandwidth greater than 1 kHz, the measurement error shall be less than 1%. This shall be true when the resistor is connected to any voltage between $V_{SS}$ and $V_{DD}$, for all operating conditions, while applying pattern P3 (see 7.3.2) to the pin and pattern P0 to all other function pins. Parasitic impedance values that are documented (see 10.2) or that can be measured via AT1 and AT2 without involving any function pins may be used to adjust the measured value before calculating the measurement error. (See 9.6.)

(h) When delivering a 1 kHz sinusoidal current of 100 µA amplitude to a function pin, and measuring the voltage via AT2, using a voltmeter with a -3 dB bandwidth greater than 1 kHz, the measured voltage shall vary by no more than 1 mV over a time interval of 1 sec.

(i) When an ATAP pin is not specified elsewhere in this standard to be connected to $V_{H}$, $V_{L}$, $V_{G}$, AB1, AB1N, AB2, or AB2N, the resistance measured between the ATAP pin and the $V_{G}$ pin, for any applied voltage between $V_{DD}$ and $V_{SS}$ shall be greater than 2 MΩ, and the capacitance shall be less than 10 pF.

(j) When an ATAP pin is not specified elsewhere in this standard to be connected to $V_{H}$, $V_{L}$, $V_{G}$, AB1, or AB2, the resistance measured between AT1 and AT2, for any applied voltage between $V_{DD}$ and $V_{SS}$, shall be greater than 20 MΩ, and the capacitance shall be less than 1 pF. If the differential ATAP pins (AT1N and AT2N) are provided, the same resistance and capacitance limits shall apply between AT1 and AT2N, between AT1N and AT2, and between AT1N and AT2N.

NOTE - It is desirable to separate AT1 from AT2, and AT1N from AT2N, with at least one other pin, so that they are not adjacent. This minimizes coupling between these pins, and also helps separate the board traces that connect to them. Minimizing the coupling between these lines facilitates the measurement of small impedances.

Recommendations

(k) If the chip has differential pins and does not have the optional pins AT1N and AT2N, then the AT1 switch path resistance ($R_{sw1}$) should be the same as the AT2 switch path resistance ($R_{sw2}$).

(l) If the transmission gate switch resistance of AT1 and AB1 is less than that specified in (a), or if the current carrying capability of AT1 and AB1 is more than that specified in (e), while achieving the requirements of all other rules, then the current limit should be documented so that a user of the component may use larger stimulus current to achieve greater accuracy for some measurements.

(m) Any buffers used in the AT1/AB1 or AT2/AB2 paths should have less than ±0.5% gain
variation between 10 Hz and 10 kHz (implying a -3 dB bandwidth of 100 kHz for a first order, low pass filter).

NOTE - Users may need to characterize gain at each measurement frequency.

9.5 Measuring performance

9.5.1 Delivering a defined current stimulus

In making measurements to verify conformance to the rules contained in this standard, a common prerequisite is the ability to deliver an accurate current stimulus. Many practical circuits for applying a known stimulus current are available in the literature. The two circuits below illustrate two different approaches.

The first method for delivering a current stimulus is to use a voltage-to-current converter, such as the one shown in Figure 40. With this circuit, it is important to observe that the only significant current paths allowed between the CUT and the current-generating circuit in the ATE are the output from the operational amplifier and the current return to its inverting input. The common node \( V_{\text{COM}} \) must be electrically isolated from the CUT, which implies that the CUT must have completely separate power supplies, with no common ground connection between the ATE, the CUT, and the measurement common ground.

![Figure 40: Applying dc + ac current to AT1](image)

The current delivered by the operational amplifier is independent of the voltage at AT1 or across the CUT, and is given by
Figure 41: Alternative circuit for applying dc + ac current to AT1

An alternative technique is to use a voltage source with non-zero output impedance and to monitor the current that the source delivers into AT1, as shown in Figure 41. This circuit delivers a specified current only into a short circuit: \( I = \left( V_{DC} + V_{ac} \right) / (R_S + R_M) \). For non-zero load impedance, the delivered current can be determined by measuring the voltage across \( R_M \). The maximum voltage swing at AT1 is independent of the CUT, however, the delivered current must be monitored or calculated to ensure that it does not exceed 100 μA.
When measuring a small inductance in parallel with a resistance, any dc offset in the stimulus voltage will cause the inductor current to quickly ramp up (or down) until it all dc current flows through it. This might affect the measurement accuracy.

$V_{DC}$ represents a dc offset voltage when the external impedance (the CUT) is purely reactive. $R_s$ represents the source impedance of the signal voltage (typically 50 $\Omega$). $R_M$ is a resistor used solely for monitoring the stimulus current (differentially).

### 9.5.2 Explanations of the rules

The following paragraphs explain the rationale behind each of the rules in 9.4, and the recommended method to verify that a component is compliant with these rules.

#### 9.5.2.1 Rule 9.4(a)

The maximum value for the switch resistance limits the stimulus current that can be applied to a CUT, and limits the voltage that can be developed across a CUT. The measurement of the internal resistances of the switch networks is a matter of applying appropriate test signals and bias conditions to the designated pins, and measuring the resulting voltages.

**Figure 42 : Measurement of $R_{sw1}$**

Figure 42 shows a circuit for measuring the switch path resistance specified in this rule. The measurement applies a stimulus current $I_{ac}$ of 100 $\mu$A peak amplitude at 1 kHz, and a bias voltage $V_{APP}$ such that

$$V_{SS} \leq V_{APP} \leq V_{DD}.$$

The switch path resistance is then given by

$$R_{S5} + R_{SB1} = V_{ac} / I_{ac}.$$
This value includes the resistances of S5 (in the TBIC), SB1 (in the ABM), $R_{com}$ (see Figure 39) and the associated wiring. The worst accuracy occurs when the bias voltage is mid-way between $V_{DD}$ and $V_{SS}$; for this case, with 100 mV across the off-chip impedance being measured, the voltage across the switches will be: \(((V_{DD} - V_{SS})/2) - 100 \text{ mV}\). Thus, the maximum switch impedance will be this voltage divided by the stimulus current (100 µA).

9.5.2.2 Rule 9.4(b)

A circuit for verifying the AT2 path switch impedance is similar to that for rule 9.4 (a), and is shown in Figure 43.

![Figure 43: Circuit for measuring $R_{sw2}$](image)

The impedance of the voltmeter is the dominant consideration in measuring the voltage at AT2. However, the bandwidth of the AT2 path is determined by both the impedance of the path from a function pin to AT2, and the total capacitance between AT2 and ground. For this reason, the path’s impedance should be as small as possible. For consistency with rule 9.4(a), and recognizing that there is no component area advantage to using a larger impedance, the maximum impedance was set to 10 kΩ. To achieve a −3 dB bandwidth of 100 kHz with this maximum switch impedance, the capacitive load on AT2 must be less than 160 pF.

9.5.2.3 Rule 9.4(c)

The output impedance of the function pin when driving $V_H$ and $V_L$ will typically be the output impedance of the normal function driver (e.g. an amplifier), and the off-chip impedances will have proportional values. When the normal function driver is not used to drive $V_H$ and $V_L$ (e.g. because its internal circuitry is not economically alterable), then separate switches can be used to deliver $V_H$.
and $V_L$. To maximize the probability that these output states will be useful, and that the test time will be reasonably short, a maximum impedance is specified consistent with rules 9.4(a) and (b). Circuits for verifying the switch impedances are significantly different from that for rule 9.4(a), and are shown in Figure 44.

![Circuits for measuring switch path impedances](image)

Figure 44: Circuits for measuring switch path impedances

9.5.2.4 Rule 9.4(d)

When measuring an impedance between two function pins having ABMs, as seen in Figure 33, there will be three switches in series with the impedance being measured: SB1, S5, and SG. The maximum resistance for $R_{SG}$ is specified the same way that the maximum resistance of SB1 and S5 is specified in 9.4(a), for the same reasons. The circuit for verifying the switch impedance is shown in Figure 45. The impedance is measured between a function pin and the pin which is declared to be $V_G$ (which might be $V_{DD}$ or $V_{SS}$).

9.5.2.5 Rule 9.4(e)

![Measurement of $R_{SG}$](image)

Figure 45: Measurement of $R_{SG}$
The basis for most of the rules in 9.4 is the assumption that 100 µA is a sufficiently large stimulus current for accurate measurements with present day impedance measurement instruments. The function pin capability is verified directly when current buffers are used, whereas rules 9.4(a)-(d) verify this indirectly when transmission gates are used. The gain of the current buffers could be any value in theory, but to ensure a usable signal-to-noise ratio, the permissible gain range is limited to be within a factor of two relative to unity. A circuit which verifies this rule is shown in Figure 46. It is important that the gain of this path be the same as that in the path AT1-AB1-AT2 to allow correction for non-unity gain (see 9.6.2 Non-characterizable errors).

![Figure 46: Measurement of current buffer performance](image)

9.5.2.6 Rule 9.4(f)

The voltage chosen to correspond to 100 µA is that for a 1 kΩ resistor, which is the geometric mean value for the target range 10 Ω to 100 kΩ. The gain of the voltage buffers is constrained to be less than unity, by the need to convey a signal of amplitude equal to $V_{DD} - V_{SS}$ from a function pin to AT2, and by the need for the gain in all pin-AB2-AT2 paths to be equal to that in the path AT1-AB2-AT2. A circuit which verifies this rule is shown in Figure 47. It is important that the gain of this path be the same as that in the path AT1-AB2-AT2 to allow correction for non-unity gain (see 9.6.1).
9.5.2.7 Rule 9.4(g)

This rule ensures that the accuracy objective for this standard is met without explicitly knowing all the potential sources of error. The measurement is performed when the function pin is programmed to pattern P3 (see Table 6) which connects only AB1 and AB2 to the function pin. Other pins must be set to their isolated state (pattern P0) to avoid the many possible combinations of output values, and to emulate the way measurements will be performed in a system (in system-level testing, one other pin might be also be connected to $V_G$). Potential sources of measurement error are described in 9.6.1 and 9.6.2, including suggestions for minimizing the impact of these errors. A circuit that verifies this rule is shown in Figure 48.

Rule 9.4(h)
This rule requires that, when the ABM is programmed to apply $V_G$ to a function pin, the voltage actually delivered to the pin is stable over the time required to make a set of related measurements. This is necessary because the voltage across a circuit element is computed by measuring (in sequence) the voltages at either end of the element with respect to $V_G$. $V_G$ itself is externally supplied, and can therefore be expected to be unvarying, but the voltage appearing at the function pin will be different, depending on the switching circuitry employed. In particular, if a method such as that illustrated in Figure 35 is employed, it is important to ensure that the voltage delivered to the function pin does not display undue variations over time.

By feeding 100 µA into the function pin, with the return to $V_G$, we can make a series of measurements (through AT2) of the voltage at the function pin, and check its variation over time. The 1 mV value corresponds to 1% of the voltage that would appear across a 1 kΩ resistor with 100 µA flowing through it. A suitable measurement circuit is shown in Figure 49.

9.5.2.8 Rules 9.4 (i) and (j)

At the board-level, it is assumed that component ATAP pins that are not involved in a test will have an impedance that is high enough not to affect the test measurements. Ideally, the impedance would be infinite, but, realistically, finite impedance will be produced by pin capacitance and protection diode leakage. Calibration of the ATAP buses can only account for non-infinite impedance if the measurement equipment has a sufficiently large dynamic range. Rules 9.4(i) and (j) are intended to ensure that the required dynamic range is reasonable for most production test equipment.

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When all 1149.4-compliant components on a board are attached to a board-level AT1/2 bus and each of them is in a state that disconnects it from AT1 and AT2, then AT1 and AT2 are not driven by the components and the voltage of these buses is intentionally unspecified in this standard so as to avoid bus contention. If the AT1 and AT2 buses are left floating in mission mode, however, they may result in noise coupling between components or be susceptible to ESD. If this is a concern, it is recommended that the user of 1149.4-conformant components (i.e. the board designer) provide means to clamp AT1 and AT2 to some dc voltage when test mode is not active. Clamping could be accomplished in a variety of ways, including jumper wires or resistors, or 3-state bus drivers.

9.6 Calibration and errors

Given sufficient measurement time, even very low voltages can be measured accurately; however, some systematic measurement errors will occur due, for example, to leakage currents. Some leakage currents can be measured and accounted for, while others cannot be measured separately. For example, current leakage in AT1 and AB1 can be measured by opening all ABM switches, and all TBIC switches except those in the component of interest. The stimulus current subsequently delivered to an ABM may then be adjusted so that the required stimulus current reaches the CUT. For currents that can be compensated, they can only be compensated while all voltages are between $V_{DD}$ and $V_{SS}$.

9.6.1 Characterizable errors

The parasitic impedances to be measured are illustrated in Figure 50.

Some of the systematic sources of measurement error that can be characterized or calibrated, and accounted for when measuring a CUT, are:

- AT1 impedance to ground, including stray capacitance, dc leakage current, etc., and also including the effects due to the ATE.

This may be measured by driving an ac + dc current into AT1, while a known resistance is connected from the ATE's AT1 pin to ground, and measuring the voltage at AT1, while ensuring that all TBIC switches are open and that the voltage is in a valid range for the AT1 pin. The impedance measured is a combination of the AT1 impedance to ground and the known resistance to ground.
Figure 50: Measurement of parasitic impedance

- AT2 impedance to ground, including stray capacitance, dc leakage current, etc., and also including the effects due to the ATE.

This may be measured by driving an ac + dc current into AT2, while a known resistance is connected from the ATE's AT2 pin to ground, and measuring the voltage at AT2, while ensuring that all TBIC switches are open and that the voltage is in a valid range for the AT2 pin. The impedance measured is a combination of the AT2 impedance to ground and the known resistance to ground.

- AB1 impedance (capacitance, dc leakage current, etc.) to ground.

This may be measured by driving an ac + dc current into AT1, while a known resistance is connected from the ATE's AT1 pin to ground, and measuring the voltage at AT2, while enabling AT1-S5-AB1-S8-AT2 on one component and disabling the TBIC switches on all other components. The impedance measured is a combination of the AT1 impedance to ground (measured separately), the AT2 impedance to ground (measured separately), the known resistance, and the AB1 impedance to ground.

- AB2 impedance (capacitance, dc leakage current, etc.) to ground;

This may be measured by driving an ac + dc current into AT1, while a known resistance is connected from the ATE's AT1 pin to ground, and measuring the voltage at AT2, while enabling AT1-S5-AB1-S8-AT2 on one component and disabling the TBIC switches on all other components.
The impedance measured is a combination of the AT1 impedance to ground (measured separately), the AT2 impedance to ground (measured separately), the known resistance, and the AB1 impedance to ground.

- **Voltage buffer gain**

When voltage buffers are used within the component for the AB2/AT2 path, the gain may be measured similarly to the method in rule (g), except that the resistor measured is connected to AT1 instead of a function pin. The gain is the ratio of the ac voltage observed at AT2 to the voltage observed at AT1, when using a high impedance voltmeter, and enabling the AT1-S7-AB2-S6-AT2 path. This does not, however, characterize any buffers used for the function pin ABM switches (see 9.6.2 Non-characterizable errors).

- **Current buffer gain.**

When current buffers are used within the component for the AB1/AT1 path, the gain may be measured similarly to the method in rule (g), except that the resistor measured is connected to AT2 instead of a function pin. The gain is the ratio of the ac voltage observed at AT2 to the ac stimulus current delivered into AT1, divided by the resistor's value, when using a high impedance voltmeter, and enabling the AT1-S5-AB1-S8-AT2 path. This does not, however, characterize any buffers used for the function pin ABM switches (see 9.6.2 Non-characterizable errors).

- **$V_{TH}$**

The threshold voltages used as a reference by the comparator in each ABM can be determined by monitoring the voltage at each pin, via AB2 and AT2, and the relevant ABM register bit value captured and shifted out during boundary scan. This method is only applicable when the voltage at the pin of interest is not varying significantly.

Note that the above measurements are described assuming a current-based driver such as that in Figure 40. The measurements can also be performed using a voltage-based driver such as that in Figure 41.

### 9.6.2 Non-characterizable errors

Some parameters of the mixed-signal test infra-structure are not measurable after the component has been embedded in the application circuit board because the external circuitry connected to the function pin will influence any measurement of the on-chip parameters unpredictably. These
parameters include primarily the characteristics of the switches connecting each pin to \(V_{IP}, V_L, V_G, AB1,\) and \(AB2.\)

Some of the sources of measurement error which cannot be characterized via \(AT1\) and \(AT2\) alone, after a component has been connected to a system, are:

- Differences in current gain between function pins, for the \(AT1\) to \(AB1\) to function pin path;

  The gain is assumed to be equal to that measured (characterized) for \(AT1\) to \(AB1\) to \(AT2.\)

- Differences in voltage gain between function pins, for the function pin to \(AB2\) to \(AT2\) path.

  The gain is assumed to be equal to that measured (characterized) for \(AT1\) to \(AB2\) to \(AT2.\)

- Differences between the expected (default or documented) value of each function pin's \(R_{com}\) and the true value (see Figure 39(b)).

- Differences between the expected (default or documented) value of each function pin's impedance to ground and the true value (see Figure 50).

- Non-linearity in the gain of the test access paths.

This may be caused by variation in the resistance of transmission gate switches: typical variation is

![Figure 51: Variation of resistance with voltage for typical transmission gate switch](image-url)
shown in Figure 51. Reducing the ac voltage or current amplitude can reduce non-linearity, but also decreases the signal to noise ratio.

- **Noise;**

Integrating over a longer period of time can reduce thermal and switching noise to arbitrarily low values. 1/f noise can be reduced by measuring at frequencies greater than 100 Hz.
10 Conformance and Documentation

10.1 Conformance

10.1.1 Specification

Rule

(a) A component claiming conformance with this standard shall comply with all the rules set out herein.

NOTE 1 - By virtue of the rules contained in 4.1, this requires that the component shall also comply with the majority of the rules of IEEE Std 1149.1.

NOTE 2 - In accordance with the rules of IEEE Std 1149.1, a component may be supplied with one or more compliance-enable pins such that full compliance with the rules of this standard is assured only when a defined pattern of enable signals is applied to the compliance-enable pin(s).

NOTE 3 - There may be more than one compliance-enable pattern.

10.2 General documentation

To allow the user to make use of the facilities included in a component, a range of information has to be made available by the manufacturer. This clause identifies the minimum data that must be provided for a component that conforms to this standard.

10.2.1 Transmission pathways

A key function of the structures described in this standard is to apply voltages and currents to function pins. This involves the use of switch pathways which, in practice, will be imperfect. The characteristics of these pathways can be defined by a model, together with the limits of operating conditions under which the model is valid.

Figure 52 shows a model that will be used to describe each of the switch pathways supplying a voltage ($V_H$, $V_L$, or $V_G$) to a function pin through its ABM. Note that the model takes no account of residual elements that remain connected to the function pin while in test mode; these are described separately.

In this model, which is intended to provide a good first-order approximation to the behavior of the pathway over a stated range of operating conditions, the supplied voltage (any of $V_H$, $V_L$ or $V_G$) is
referred to a particular power/ground supply pin with a defined offset voltage $V_{\text{Offset}}$ and with an injected leakage current $I_{\text{Leak}}$. The impedance of the pathway, $Z$, includes the switch impedance(s) as well as the bus and wiring impedances. The "validity range" of the model is described in terms of the current through the pathway ($I_{\text{Path}}$) and the voltage across it ($V_{\text{Path}}$), which must lie between defined limits if the model is to be a reasonably accurate representation of the actual behavior.

![Figure 52: Model for switch pathway](image)

Each switch pathway in the ABM can then be represented by a 10-valued vector of model parameters containing:

1. The names of the "From" and "To" pins. This defines the conventional direction of current flow (from the "From" pin towards the "To" pin).
2. The minimum and maximum path impedance in ohms of the path between the pins.
3. The minimum and maximum voltage offset along the path (which may be zero).
4. The minimum and maximum current leakage injected into the path (which may be zero).
5. The minimum and maximum value of the voltage between the "From" pin and the "To" pin for which this model is valid.

**NOTE** - If one of these voltage values is negative, it would imply that the source connected to the "From" pin could sink current as well as source it, and that the switch pathway supports bidirectional current flow.
Each ABM is required to connect $V_H$, $V_L$ and $V_G$ to its function pin by way of switch pathways, each of which will be described in terms of the 10 parameters associated with the model. The same model can also be used to describe the behavior of the path from AT1 (the current-capable path) to the function pin, when both switches S5 in the TBIC and SB1 in the ABM are closed, and similarly for the path from the function pin to AT2.

Table 11 : Typical switching pathways

<table>
<thead>
<tr>
<th>“From” pin</th>
<th>Switches in pathway</th>
<th>“To” pin</th>
<th>Operating condition</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>$V_{DD}$</td>
<td>SH (ABM)</td>
<td>Function</td>
</tr>
<tr>
<td>2</td>
<td>Function</td>
<td>SL (ABM)</td>
<td>$V_{SS}$</td>
</tr>
<tr>
<td>3</td>
<td>Function</td>
<td>SG (ABM)</td>
<td>$V_G$</td>
</tr>
<tr>
<td>4</td>
<td>AT1</td>
<td>S5 (TBIC) + SB1 (ABM)</td>
<td>Function</td>
</tr>
<tr>
<td>5</td>
<td>Function</td>
<td>S6 (TBIC) + SB2 (ABM)</td>
<td>AT2</td>
</tr>
<tr>
<td>6</td>
<td>$V_{DD}$</td>
<td>S1 (TBIC)</td>
<td>AT1</td>
</tr>
<tr>
<td>7</td>
<td>AT1</td>
<td>S3 (TBIC)</td>
<td>$V_{SS}$</td>
</tr>
<tr>
<td>8</td>
<td>$V_{DD}$</td>
<td>S2 (TBIC)</td>
<td>AT2</td>
</tr>
<tr>
<td>9</td>
<td>AT2</td>
<td>S4 (TBIC)</td>
<td>$V_{SS}$</td>
</tr>
</tbody>
</table>

The first five lines of Table 11 show the pathways that need to be defined for a typical function pin. Lines 6 to 9 demonstrate how the same model is used to define the performance of the pathways associated with the AT1 and AT2 pins, which are required to be capable of delivering $V_H$ and $V_L$ to the board-level buses.

As an example, consider an ABM constructed in a 5 volt CMOS technology where the native driver is used to produce $V_H$. The 10 parameters could be:

1. from $V_{DD}$ to Function pin
2. 40 - 60 Ω
3. 0 - 0 V
4. 0 - 0 A
5. 0 - 3.5 V
NOTE 1 - For this example, if the device has an allowed range of \( V_{DD} \) values (e.g., 5 to 15 volts) then items 3, 4, and 5 in the table could be given as a proportion of \( V_{DD} \).

NOTE 2 - If the ABM used an SH switch to produce \( V_H \) rather than using the "native" driver, the impedances shown would probably be much higher. Using the "native" driver to supply \( V_H \) and \( V_L \) will usually imply a current drive capability sufficient to match the load seen by this driver as presented by external circuitry. This will allow interconnect testing to be done in the presence of loading that might prevent low-current capacity switches from achieving the same result. Test generators will need to make use of this fact.

NOTE 3 - If several function pins have identical ABM implementations, they may all share the same models and parameters, reducing the volume of data required for description.

An Automatic Test Program Generator would use this data to determine whether a given ABM was capable of delivering \( V_H \) as required by some receiving ABM elsewhere on a board through any extended interconnect.

### 10.2.2 Specification

**Rules**

(a) The documentation specified in IEEE Std 1149.1 shall be provided.

(b) The set of defined public instructions supported shall be listed, together with the corresponding instruction code(s) for each instruction.

**NOTE - Defined public instructions are those instructions defined in IEEE Std 1149.1 and in this standard listed below.**

<table>
<thead>
<tr>
<th>Instruction</th>
<th>Status</th>
<th>Instruction</th>
<th>Status</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>SAMPLE/PRELOAD</strong></td>
<td>Mandatory</td>
<td><strong>EXTEST</strong></td>
<td>Mandatory</td>
</tr>
<tr>
<td><strong>BYPASS</strong></td>
<td>Mandatory</td>
<td><strong>PROBE</strong></td>
<td>Mandatory</td>
</tr>
<tr>
<td><strong>INTEST</strong></td>
<td>Optional</td>
<td><strong>RUNBIST</strong></td>
<td>Optional</td>
</tr>
<tr>
<td><strong>HIGHZ</strong></td>
<td>Optional</td>
<td><strong>IDCODE</strong></td>
<td>Optional</td>
</tr>
<tr>
<td><strong>CLAMP</strong></td>
<td>Optional</td>
<td><strong>USERCODE</strong></td>
<td>Optional</td>
</tr>
</tbody>
</table>

(c) For each user-defined public instruction supported, other than those defined in this standard or in IEEE Std 1149.1, the following information is required.
(i) The binary code(s) for the instruction.

(ii) A list of test data registers affected by the instruction.

(iii) The name of the serial test data register path selected by the instruction to be connected between TDI and TDO.

(iv) A definition of the purpose of the instruction, the method of performing the test, the test data register(s) that will hold the results of the test, and the way in which these results are to be examined.

(d) If private instructions are utilized in a component, the vendor shall clearly identify any instruction codes that, if selected, would cause hazardous or unpredictable operation of the component.

(e) For each ABM attached to a function pin, the following data shall be supplied.

(i) The behavior of the boundary module, including signals captured by uncommitted capture flip-flop inputs used to improve ABM testability.

(ii) The positioning of the control bits within the boundary-scan register.

(iii) The value and tolerance of $V_{TH}$.

   NOTE - If there is a non-zero tolerance on $V_{TH}$, this indicates that a portion of the voltage range between $V_H$ and $V_L$ cannot be used to resolve a signal voltage into a digital bit.

(iv) A set of 10 model parameters for each of the pathways associated with $V_G$, $V_{HP}$, $V_L$, $AT1$, and $AT2$.

(f) For the TBIC, the following data shall be supplied.

(i) The behavior of the boundary module, including signals captured by uncommitted capture flip-flop inputs used to improve TBIC testability.

(ii) The partitioning (if any) of the internal test bus structure.

(iii) The number of partitions.
(iv) The allocation of ABMs to partitions.

(v) The positioning of the control bits within the boundary-scan register.

(vi) The value and tolerance of $V_{TH}$.

NOTE - If there is a non-zero tolerance on $V_{TH}$, this indicates that a portion of the voltage range between $V_H$ and $V_L$ cannot be used to resolve a signal voltage into a digital bit.

(vii) A set of 10 model parameters for each of the pathways involved with delivering $V_H$ and $V_L$ to AT1 and AT2.

(g) If a differential ATAP is included in the component, documentation relating to AT1N and AT2N shall be provided in the same form as that for AT1 and AT2 respectively.

10.3 Documentation of residual elements

10.3.1 Specification

Rules

(a) Any circuit network that remains connected to the function pins when the component is in CD mode shall be modeled as a network of residual elements, and described in a Residual Element Table.

NOTE 1 - Residual elements may be connected from function pins to power pins, other function pins, or other residual elements (see 7.3.3).

NOTE 2 - The Residual Element Table will be used to account for common series resistance in the metalization, pad, bond wire and lead frame between a device pin and the ABM ($R_{com}$ in Figure 39(b)), as well as the effects of significant capacitance to ground that may exist.

NOTE 3 - The value of $R_{com}$ always needs to be documented, since even a value of less than 1Ω can produce errors of more than 1% when measuring some impedances within the stated target range (10Ω to 100 kΩ).

NOTE 4 - If analog pins have a common design "footprint" a single general model may suffice to document the series impedance and capacitance to ground for all the analog pins. This model could be based on Figure 52, noting that, in some cases, the values of resistance may be zero and/or the capacitance may be small enough to ignore.
Figure 53: Examples of residual elements

10.3.2 Description

Figure 53 shows a component with function pins F1 - F8 (each of which could be either an input or an output pin), two power supply pins (PWR and GND), and containing a number of elements that lie outside the core circuitry.
R1 is a resistance between function pins F1 and F2, and R2 is a parallel termination to a power pin from function pin F3. R4, R5, and I1 can be seen as a network connecting function pins F5, F6, and F7, and also including an internal node (node N2) that is also external to the core circuitry.

R3 and R6 are examples of $R_{com}$. These elements introduce internal nodes N1 and N3 that differ from N2 in that they are directly connected to ABMs. This requires an additional notation in the Residual Elements Table (the “(ABM)” notation) so that the appropriate ABM can be identified. C1 represents the capacitance to Ground from the internal node N3.

Table 12 : Residual element table for the component shown in Figure 53

<table>
<thead>
<tr>
<th>Label</th>
<th>Units</th>
<th>From</th>
<th>To</th>
<th>Min</th>
<th>Max</th>
<th>Match/correlate</th>
</tr>
</thead>
<tbody>
<tr>
<td>R1</td>
<td>Ohms</td>
<td>F1</td>
<td>F2</td>
<td>90</td>
<td>110</td>
<td></td>
</tr>
<tr>
<td>R2</td>
<td>Ohms</td>
<td>F3</td>
<td>PWR</td>
<td>30</td>
<td>40</td>
<td></td>
</tr>
<tr>
<td>R3</td>
<td>Ohms</td>
<td>N1</td>
<td>F4</td>
<td>30</td>
<td>40</td>
<td></td>
</tr>
<tr>
<td>(ABM)</td>
<td></td>
<td>N1</td>
<td>F4</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>I1</td>
<td>Amps</td>
<td>N2</td>
<td>F5</td>
<td>$2\times10^{-7}$</td>
<td>$3\times10^{-7}$</td>
<td></td>
</tr>
<tr>
<td>R4</td>
<td>Ohms</td>
<td>F6</td>
<td>N2</td>
<td>120</td>
<td>140</td>
<td>R5/0.95</td>
</tr>
<tr>
<td>R5</td>
<td>Ohms</td>
<td>F7</td>
<td>N2</td>
<td>120</td>
<td>140</td>
<td>R4/0.95</td>
</tr>
<tr>
<td>R6</td>
<td>Ohms</td>
<td>N3</td>
<td>F8</td>
<td>30</td>
<td>40</td>
<td></td>
</tr>
<tr>
<td>C1</td>
<td>Farads</td>
<td>N3</td>
<td>GND</td>
<td>$1\times10^{-11}$</td>
<td>$2\times10^{-11}$</td>
<td></td>
</tr>
<tr>
<td>(ABM)</td>
<td></td>
<td>N3</td>
<td>F8</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

NOTE 1 - Three internal nodes N1 - N3 are part of this network, isolated from the core by the core disconnect function. N2 is an independent node, not directly connected to an ABM.

NOTE 2 - Nodes N1 and N3 are connected to ABMs, and each requires an additional (ABM) entry in the label column to identify the node with its ABM. In this case, the “from” field identifies the internal node connected to the ABM, and the “to” field identifies the ABM by its function pin.

NOTE 3 - The current source $I$ has polarity, so the “from” and “to” fields are used to indicate the direction of current flow through the source.
Residual elements are those that cannot be disconnected from the pins by the core disconnect function, and that therefore must be documented in a Residual Element Table. This table also, as a matter of convenience, includes elements that lie in series between the ABM and the pin (such as $R_{com}$ in Figure 39(b)): such series impedances are often associated with ESD protection circuitry and bond wires. Some portion of ESD protection circuitry (such as reverse-biased clamp diodes) do not need to be documented because they will not conduct current during normal testing activities; series impedances will need to be documented.

Each element, regardless of how it is implemented, must be characterized by a model containing only R, L, C, and independent V and I elements.

The match/correlation field for a particular element may be empty, or it may contain a list of element identification labels that are matched to this element, along with a specified correlation between -1.0 and +1.0. This is used to identify groups of residual elements whose values are matched such that their variations (between min and max) are correlated and not independent.

The residual element table for the component of Figure 53 is shown in Table 12.