ABIS
Analog BIST for Integrated Systems

The team
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The Background
System level integration is evolving as a new paradigm in system design, allowing an entire system to be built on a single chip. However, once these cores are connected together their testing is challenged by the structural and functional complexity of the resulting chips. According to the “The International Roadmap for Semiconductors” efforts should be put on the development of BIST (Built-In Self Test) and DfT (Design for Testability) methodologies which allow to perform reliable, yet economic, tests all over the life cycle of the product.

The Objective
This project aims the development of two IP cores according the specifications of the IEEE P1500 Embedded Core Test WG:
- a BIST wrapper for A/D converters
- a dedicated processor to control the test framework within the integrated system where the A/D converter is placed

The dedicated test processor controls the test infrastructure used to access all test resources embedded within the integrated system chip, and performs core testing together with the respective BIST and DfT schemes, particularly with the ADC BIST wrapper. This way various test resources can be reused to perform different test operations.

The test wrapper for A/D converters provides: stimuli generation, input/output partitioning for control and observation, response capture, time synchronism, adjacent testability, and local processing. It incorporates four modes of operation: normal, core-internal / - external test, and isolation.

Previous work